On-Wafer Measurement and Modeling of Silicon Carbide MESFET's

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Abstract **–** The goal of this work was to characterize Silicon Carbide (SiC) transistor devices, with measurements and modeling using an advanced software package. To characterize and model the SiC Metal-Semiconductor Field-Effect Transistors (MESFETs), on-wafer measurements of the transistors were performed and their behavior was characterized. The transistors were measured using a vector network analyzer in conjunction with a probing station to make contact with the individual devices on the wafers. Once measurements were complete and typical performance characteristics found, equivalent circuit models were designed and the components optimized to create equivalent circuits with matching characteristics.

Keywords: Silicon carbide, MESFET, on-wafer measurements, and optimization.

I. ON-WAFER MEASUREMENT OF SIC TRANSISTORS

A study of a Silicon Carbide transistor behavior was performed using a variety of different transistors on a fabricated wafer. Silicon Carbide transistors, because of their high temperature capability, are expected to be used for high power devices in the future. The Silicon Carbide MESFET's were made using a proprietary process, and one goal of this research was to supply performance characteristics of these transistors so that further refinement and enhancement of the fabrication process could be achieved. The transistors were measured using the Agilent 8510C vector network analyzer (VNA), the Cascade Microtech Summit 9000 probing station, and several Agilent DC power supplies and multimeters. The small-signal measurements were made, with the operating point for each device typically chosen in the saturation (active) region of the devices. From these measured results, an analytical characterization using curve fitting and a numerical characterization using optimization of the microwave transistor were obtained. In addition, for the curve fitting procedure, a measurement was made with the device in the "cold" or pinched off region. The measurements were performed in the frequency range from 0.1 to 8 GHz with 201 frequency points; with the calibration of the network analyzer completed using the SOLT (short-open-load-through) method. The calibration substrate used for successful calibrations was included with the Cascade Microtech probe station and designed for the appropriate size probe pitch, 100 μm pitch for these measured transistors. A sample wafer from the fabrication company is shown in Fig. 1, below.

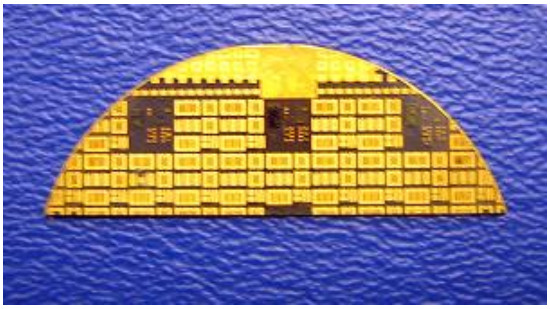

Fig. 1. Typical silicon carbide wafer measured and modeled.

The wafer was composed of several different sizes of transistors as seen on the left in Fig. 2, each with its individual DC curves for choosing an appropriate operating point. Several types of transistors with different sizes are shown in Fig. 2, with the gate, drain, and source labeled as compared to a typical transistor symbol [1].

The wafer was composed of several different sizes and types of transistors, each with its individual DC curves for choosing an appropriate operating point. An example of these curves is shown below in Fig. 3. The transistors measured were n-channel depletion mode devices, and therefore the gate voltage must be kept negative with respect to the drain voltage for operation in the active region [2]. In the DC characteristics, the different colored curves represent values of V_{GS}, the voltage from the gate to the source. For the shown curves, V_{GS} varies from -7 Volts to 1 Volt. The V_{GS} curves are plotted as functions of V_{DS}, the voltage from the drain to the source, versus I_D, the current through the drain.

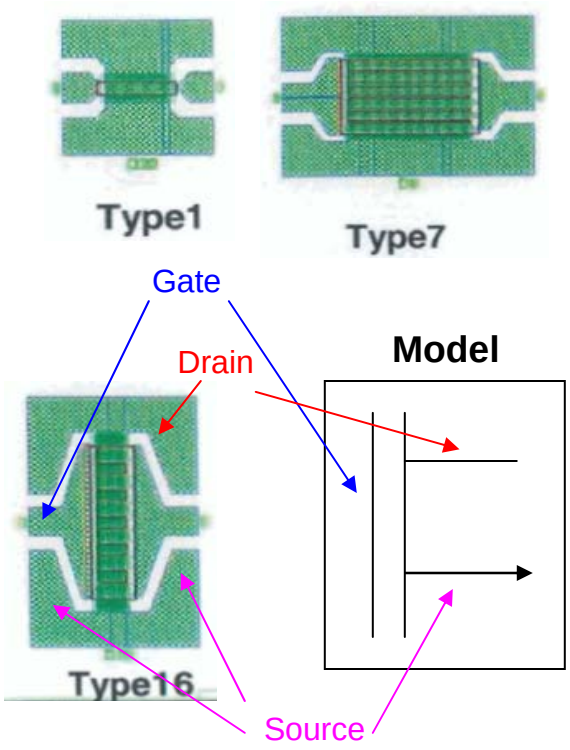

Fig. 2. Different transistor types compared along with typical MESFET symbol.

II. DATA DISPLAY

Once measurements were completed using the VNA, useful RF characteristics for each device were computed and provided to the manufacturer. Typical performance characteristics such as the gain and stability of the transistor are displayed in Fig. 4.

These characteristics are obtained from the measured S-parameters; the measured S-parameter data is processed through simulation in Agilent's Advanced Design System (ADS) to provide the useful characteristics [3]. The stability is shown in terms of the μ-factors, both required to be above unity for unconditional stability, and in terms of the K-factor, also required to be above one for stability [4]. The maximum gain in decibels is also given, with these results shown at 1 GHz and 2.4 GHz. These frequencies were chosen for display because they are in the GPS, wireless local-area network, WLAN, and WiMAX frequency bands. They are also typical operating frequencies for which Silicon Carbide transistors expect to be utilized. The S-parameters are displayed in the Smith Chart format for the input and output reflection coefficients, S_{11} and S_{22}, and are shown in decibels as functions of frequency for the amplitude of the forward transmission S_{21} and the reverse transmission S_{12}.

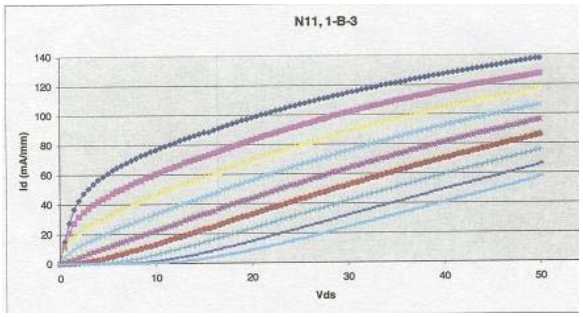

Fig. 3. DC characteristic curves.

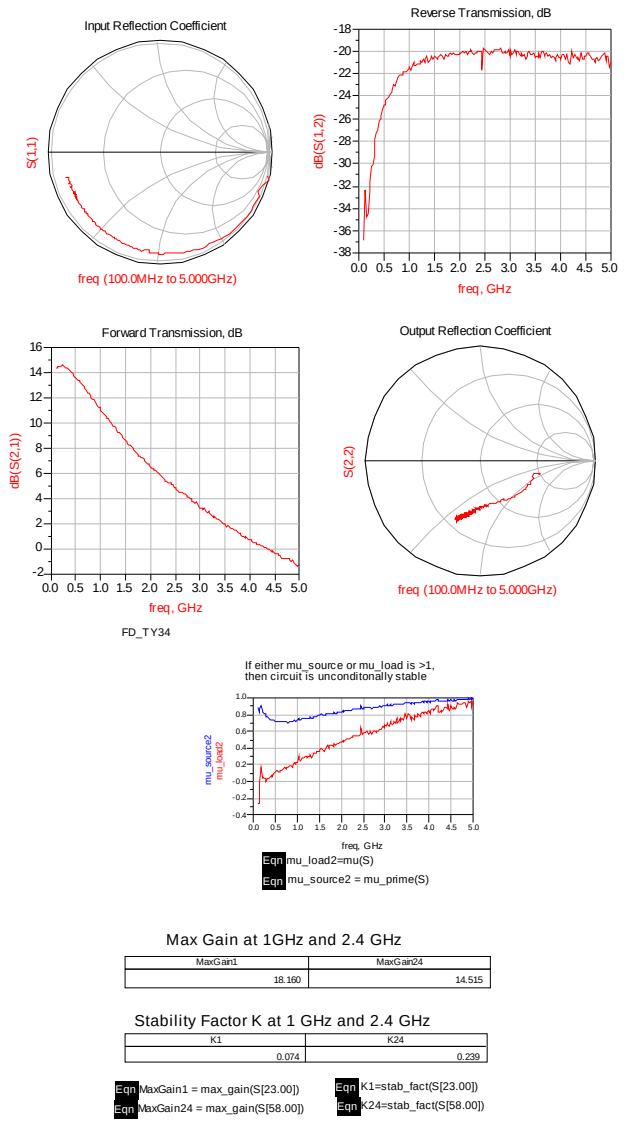

Fig. 4. Typical performance characteristics of a SiC device.

III. EQUIVALENT CIRCUIT MODELING

With the measurements completed, a conventional small signal equivalent circuit was used to find the values of the individual elements in the circuit. An advantage of finding a matching equivalent circuit for each transistor is the insight it provides into the correlation between each element to its physical dimension on the actual device. Therefore the equivalent circuit model can be used to possibly make improvements in the design of the transistor. The equivalent circuit can also provide helpful information for the device performance analysis, such as gain and noise [5]. It also can provide an estimate of results in a greater frequency range, if the measurement equipment is not capable of measuring the entire range needed [6].

The individual elements in the equivalent circuit were first found using two techniques: an analytical procedure which utilized curve fitting and required two measurements, one with the device "off" and another with the device "on", and an optimization procedure which only required one measurement. The equivalent circuit layout used, a common source configuration, is shown in Fig. 5 [7], with the gate, drain and source labeled as G, D, and S, respectively. This is a typical model for any FET. Other models could be used, but the capacitors and resistors in this model correlate well with the physical characteristics of the transistor.

Initially only the internal elements, shown in the red box, were used to find the equivalent circuit for both procedures. For several of the smaller transistors, this was all that was needed to create matching S-parameters of the model with the measured results. For the larger transistors, the external elements, which are the extrinsic parasitic elements, were added for a more accurate model. These external elements, independent of biasing [8], represent the finite length of the metallic strip between the probe tips and the semiconductor device and account for the parasitic capacitance and series inductance and resistance associated with the metal to metal contact. The leads of packaged devices can also attribute to the parasitic elements and can be represented in the external elements. In the layout in Fig. 5, each internal element is as follows: C_{GD}: gate-to-drain capacitance, C_{GS}: gate-to-source capacitance, C_{DS}: drain to source capacitance, R_{GS}: small gate-to-source channel resistance (charging resistance of C_{GD}), R_{DS}: drain to source resistance and Gm: transconductance. Tau is not shown in the layout but is an element of the equivalent circuit included in the voltage controlled current source, and it is the electron transit time through the channel. The capacitances $C_{GD,}$ C_{GS}, and C_{DS} are created from the small gaps between the gate, drain and source on the physical transistor itself. The gain of the device is produced by the dependent current generator, which depends on the voltage across $C_{GS,}$ leading to $|S_{21}| > 1$. The reverse signal path, S_{12}, is controlled solely by C_{GD} and is typically very small [9].

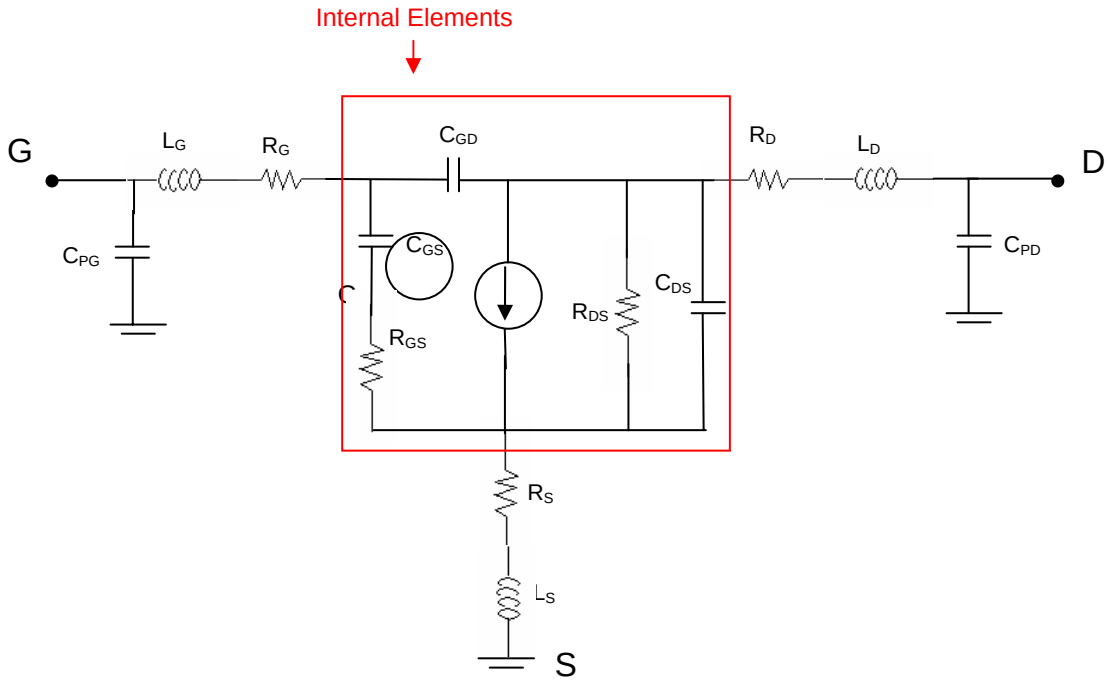

Fig. 5. Transistor equivalent circuit.

This layout was created in the schematic shown in Fig. 6 using ADS, and the elements were optimized to create matching S-parameters to the measured results. Originally, the values obtained from the curve fitting procedure were entered as a starting value, and the optimization proceeded to better fit the curves. The optimization was also run starting with random numbers (but still within a reasonable range), and it reached the same goal, confirming the accuracy of the optimization procedure. A conjugate gradient optimization was used to find the local optimum point, and then a random optimization was utilized to make sure that the minimum was not just a local minimum. One important thing to note about the optimization procedure is that it takes into account the effects of the interaction between the different elements. It simulates the circuit as a whole, whereas the curve fitting technique only analyzes the individual elements or a couple of them at a time. Therefore the efficiency and accuracy of the optimization eliminates the need for the more time-consuming linear curve fitting technique for each transistor. An initial estimate based on experience can be accurate enough for the optimization procedure to reach its optimal values [10]. The goal of optimization was to minimize the difference between the measured and simulated curves of all four S-parameters, each with equal weights. The analytic values were also used in a separate schematic and held constant for comparison. The results show the optimized results being the closer match, but all three, measured, analytic, and optimized, were similar.

Shown in Fig. 6 is the full equivalent circuit schematic used for the larger transistors. Parasitic series inductances and resistances and shunt capacitances were added to the gate and drain, and at the source, a series combination of inductance and resistance.

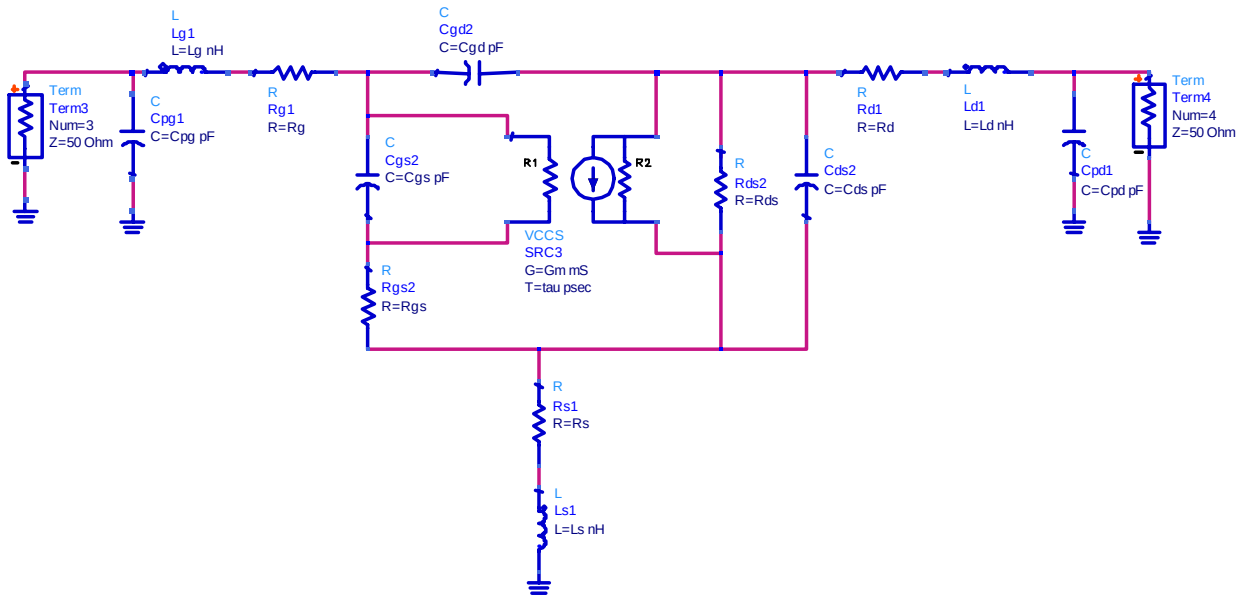

Fig. 6. Layout of equivalent circuit with external elements.

IV. RESULTS

The results for two different transistors, a small one and a large one, are included in tables listing the different element values and also in the form of the S-parameters plotted on Smith Charts. In Table 1, the elements from the small transistor are listed with the analytic values and the optimized values, with the percentage difference included in the last column. The difference is typically around 3%, indicating good agreement of the analytic procedure with the optimization. The reason for the larger percentage difference for C_{DS} is unknown; however, the optimized results do show better accuracy and this capacitance, which is nearly five times smaller than C_{GS}, does not have the deleterious effect that C_{GS} has on the performance of a common source amplifier.

Table 1. Element values for small transistor.

Small Transistor	Analytic	Optimized	Percent Difference
C_{GS} (pF)	0.5424	0.530	2.29
R_{GS} (Ω)	11.4	11.82	3.68
C_{GD} (pF)	0.1936	0.1981	2.32
Gm (mS)	16.94	16.55	2.3
R_{DS} (Ω)	277.3	285.6	2.99
C_{DS} (pF)	0.1424	0.1068	25
tau (ps)	7.1576	6.6662	6.92

From the small transistor listed in Table 1, Fig. 7 contains the results from simulations with only the internal elements, and Fig. 8 is with the external elements added to the previous model, both with the measured results in green, the analytic in blue, and the optimized results in magenta. On both Smith Charts, the better fitting curve is the one simulated with the optimized element values.

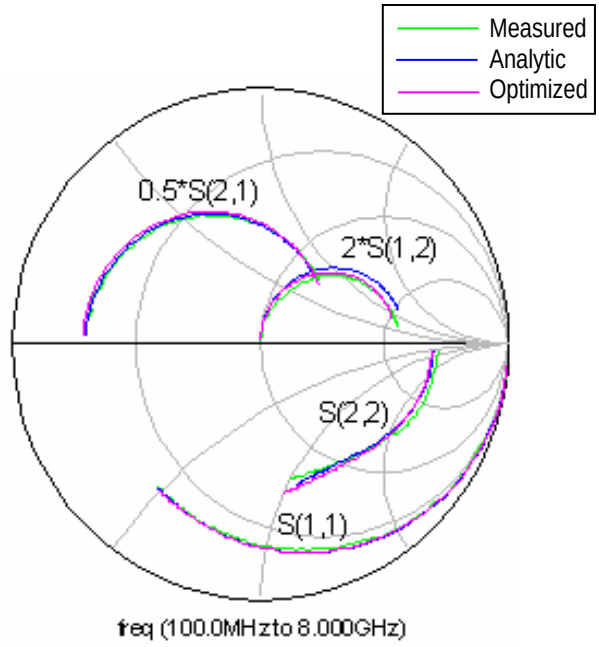

Fig. 7. Results with only internal elements.

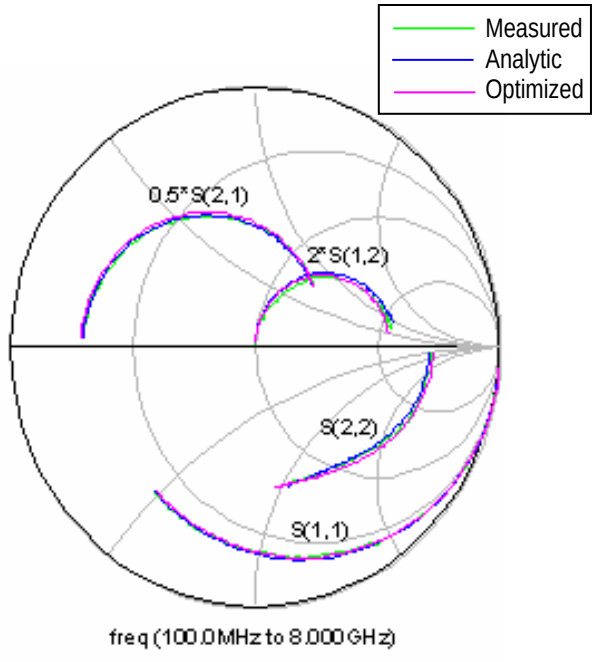

Fig. 8. Results with external elements.

In this case, the external elements create only a slightly closer match with the measured results, but the difference is not significant. As seen from these results from the small transistor, the network including only the internal elements is an accurate model for it. Therefore for simplicity, the equivalent circuit with fewer elements can be used for the small transistors.

In Fig. 9, a different, larger transistor is shown, labeled as Type 14. The top right picture is its physical layout, the larger blue picture is a layout of the die, with the red circles showing where this particular type of transistors are located, and the curves shown are the DC characteristic curves. All four of these Type 14 transistors contained on the individual die were measured with the probing station.

Table 2 below contains the optimized element values from the equivalent circuit for the Type14 transistor. The numbers, #1, #2, and #3, refer to three of the transistors measured at three different physical locations on the die, as shown in Fig. 9. The fourth transistor did not function properly and results are not shown from it. Each of the individual transistors was measured at several different bias voltages, and the bias voltages for each measurement are included in Table 3.

As seen in Table 2, the element values for each transistor vary at different bias points as the internal elements are bias-dependent [10], and they also vary between the three different transistors. These variations show the effect that DC biasing has on the intrinsic elements; different bias points produce different results. Also seen from the table is that no two transistors will produce identical results. They are similar but still not exact, as the measurement #1 (c) and the measurement #2 (a) were measured at the same exact bias voltages, but producing different results with different drain currents. Thus, to obtain a model that works perfectly for every transistor is a challenging task.

The S-parameters shown in Fig. 10 on the Smith Chart compare the measured results from one Type 14 transistor with the equivalent circuit with only the internal elements included and also with the results from the full equivalent circuit including the external parasitic elements. It can be seen that the circuit including the external elements is a better fit for this transistor, as this is one of the larger types measured and the external parasitics are more prevalent. The green curves are the measured data, the magenta is the optimized data with no external elements, and the blue curves are the optimized data with external elements. These results were typical for the larger transistors, showing that the full equivalent circuit creates a closer match for these devices and should therefore be used when modeling them. In particular, the results from the model including the external elements provide a much better match for S_{12} and S_{22} to the measured results, as the circuit with only internal elements could not produce an accurate agreement. The

optimized results for each transistor create a close match to the measured but are never exact. One possibility for inexact matching of the S-parameters is poor contact with the probe and the transistor. The wafer under test was particularly small and the vacuum system of the probe station was not efficient at holding the wafer in place, and instability of the probe tips may have occurred. This appears as "wiggles" at the upper frequency range. Overall, however, successful results were achieved, with accurate measurements and modeling.

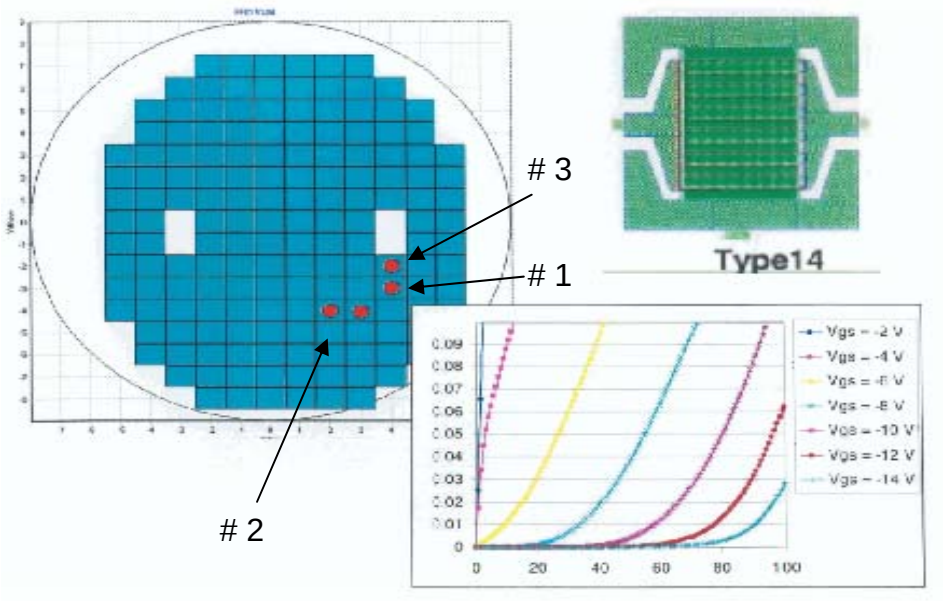

Fig. 9. Die layout, DC characteristic curves, and transistor layout.

Table 2. Element values for large transistor.

TYPE 14	C_{GS}(pF)	R_{GS}(Ω)	C_{GD}(pF)	Gm(mS)	R_{DS}(Ω)	C_{DS}(pF)	Tau(ps)
# 1 (a)	2.47389	1.26921	0.08195	66.2317	149.255	0.574277	14.5083
# 1 (b)	2.32202	1.60175	0.279425	64.9661	145.266	0.555315	14.4285
# 1 (c)	2.48972	1.21685	0.267132	76.6272	130.792	0.56288	14.3795
# 2 (a)	2.19978	0.693172	0.290189	59.5484	131.87	0.550824	13.8515
# 2 (b)	2.48747	0.528603	0.261274	79.0292	116.633	0.566017	13.898
# 3 (a)	3.1535	2.67609	0.265302	72.3178	132.464	0.657601	21.2513
# 3 (b)	3.1288	2.58207	0.222869	81.7162	124.204	0.645889	20.5984
# 3 (c)	3.57608	2.6709	0.20941	99.8517	102.227	0.676571	21.0207

Table 3. Bias voltages.

TYPE 14	V_{GS} (V)	V_{DS} (V)	I_D (mA)
# 1 (a)	-7	30	36
# 1 (b)	-7.5	48	45
# 1 (c)	-7	48	71
# 2 (a)	-7	48	54.5
# 2 (b)	-6	48	91.2
# 3 (a)	-6	20	39
# 3 (b)	-6	30	55.8
# 3 (c)	-5	25	109.1

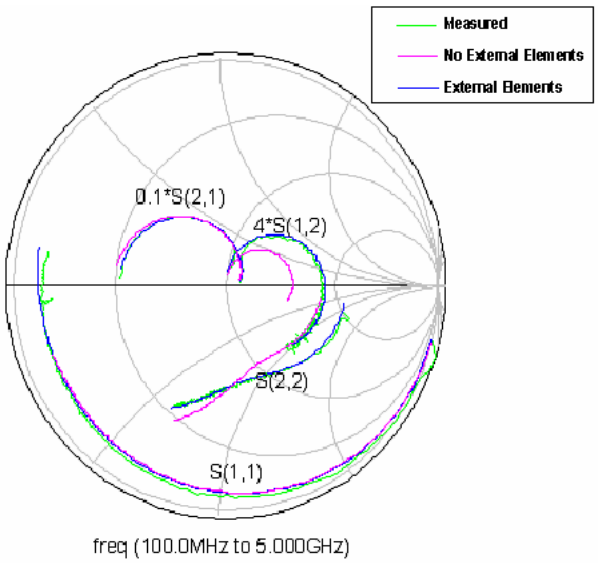

Fig. 10. Comparison of internal and external elements.

V. CONCLUSION

As seen from the above results, the optimization process yields a rather accurate model with little error for the transistor. A possible reason for this small error in inexact matching of the S-parameters is poor contact with the probe and the device under test. Some of the devices were so small that the vacuum system of the probe station was not efficient in holding the wafer in place, and instability may have occurred. In addition, it was shown that the external parasitic elements could be added to the circuit optimization with better expected results, albeit while taking more computational time.

ACKNOWLEDGMENTS

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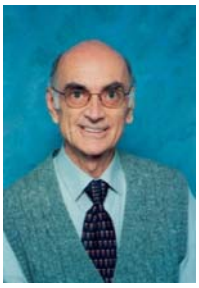

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