A 340-400 GHz Zero-Biased Waveguide Detector Using an Self-Consistent Method to Extract the Parameters of Schottky Barrier Diode

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Abstract — A type of low-barrier Schottky barrier diode (SBD), based on InGaAs/InP, is designed and fabricated, and then a 340-400 GHz zero-biased waveguide detector utilizing this diode is proposed. To predict the performance of the SBD, firstly we present a self-consistent analytical method to find the accurate values of the parameters of the SBD by using the on-wafer measured S-parameter under different bias conditions up to 40 GHz and an auxiliary de-embedding structure. The extracted values show a very good agreement with the theoretical values. Then a concept called effective capacitance is proposed to model the high frequency (340-400 GHz) properties of the SBD. This concept has greatly improved the consistency of the simulated and measured results of the detector. The measured maximum voltage responsivity and the minimum noise effective power (NEP) of the detector are 800 mV/mW and 3.46×10^{-11} W/Hz$^{0.5}$ at 382 GHz, respectively.

Index Terms — Detector, effective capacitance, InGaAs/InP, low barrier, modeling technology, parameter extraction, Schottky barrier diode.

I. INTRODUCTION

Terahertz (THz) detection technology is becoming more and more attractive for its applications in astronomy, imaging and bio-sensing [1,2].There is a number of ways to achieve THz detection [3]. Bolometers are extremely sensitive, providing responsivity up to 10^5 V/W, and noise equivalent power (NEP) about 10^{-13} W/Hz$^{0.5}$. But relatively speaking, they have a slow temporal response and require cryogenic condition [4]. A room temperature THz detector which has high responsivity, high stability, and low cost of fabrication will greatly promote the application of THz technologies. Schottky barrier diode (SBD) detectors have long been used in millimeter-wave (MMW) and THz regions because of their high sensitivity, ability to operate at an ambient or cryogenic temperature and fast response time. When the diode is optimized to have a low forward turn-on voltage, the detectors can achieve excellent frequency response and bandwidth, even with zero-bias. InGaAs/InP is verified to be a very promising material system for the detection at MMW and THz frequencies. Superior to traditional material, such as GaAs, its lower Schottky barrier height provides zero-bias detection ability that not only eliminates shot noise and hence improves crucially signal-to-noise ratio, but also simplifies the detection system [5].

In this study, a planar SBD using InGaAs/InP material system with low barrier height is designed and fabricated at Institute of Microelectronics of Chinese Academy of Sciences (IMCAS). Based on this SBD, a 340-400 GHz zero-biased waveguide detector is proposed.

The hardest and most important part of the solid-state circuit design is the modeling of the device. The deviation between the simulated and measured results is mainly due to the inaccurate modeling technique. Here, we propose a self-consistent modeling technique of SBD which is based on an analytic method to extract the parameters of SBD from the on-wafer measured S-parameter data. The extracted values of the parameters agree well with the theoretical values. Then an extrapolation process and a concept called effective capacitance are also presented, which greatly improve the consistency between the simulated and measured results.

II. DESIGN AND MODELING OF THE SBD

A common structure of a planar SBD is depicted in Fig. 1 (a). As mentioned above, detectors based on SBDs with low forward turn-on voltage can achieve excellent frequency response and bandwidth. Hence, InGaAs/InP material system which has a low barrier height is used here. The doping levels and the thicknesses of epitaxial

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layer and buffer layer need to be carefully designed to meet the demand of the detector. In order to minimize the series ohmic contact resistance, the buffer doping concentration (N_{buffer}) should be as high as possible; for instance, 3×10^{19} cm^{-3}, which is near to the upper limit of InGaAs. The thickness of buffer layer (t_{buffer}) should be larger than one skin depth at the operating frequency, but larger thickness leads to larger cost. So the trade-off value is chosen to be 1.5 μm. Both epitaxial doping concentration (N_{epi}) and epi-layer thickness (t_{epi}) should be considered at the same time. t_{epi} should be slightly larger than the maximum depletion depth, which is also relative to N_{epi}. The decision of N_{epi} is a compromise between series resistance and reverse breakdown voltage. Here, N_{epi} and t_{epi} are chosen as 2×10^{17} cm^{-3} and 0.2 μm, respectively. The diameter of the Schottky contact was chosen as 2 μm to obtain a reasonable junction capacitance which satisfies the demand of the detector at specified frequencies [6,7].

The fabrication process of the SBD is described briefly as follows. Firstly, the epitaxial lattice matched $In_{0.53}Ga_{0.47}As$ structure including a 1.5 μm thick heavily doped n^+-type buffer layer and a 0.2 μm thick n-type epitaxial layer was grown on a semi-insulating (SI) InP substrate using molecular beam epitaxy (MBE). The doping concentration of the two layers are 3×10^{19} cm^{-3} and 2×10^{17} cm^{-3}, respectively. Secondly, the ohmic contact was formed at the epi-layer by etching through the n-type buffer layer and depositing a Ti-Pt-Au metal. Thirdly, a SiO_2 layer was deposited on the epi-layer to provide passivation and insulation. Fourthly, the Schottky contact was formed by opening a current window on the insulating layer followed by depositing a metal contact on the epi-layer. Fifthly, a narrow metal connection was formed across the surface-channel to route the Schottky anode path towards a large anode contact pad. This narrow metal connection is known as the air-bridge finger. Finally, the $In_{0.53}Ga_{0.47}As$ material beneath the air-bridge finger was removed to isolate the anode and cathode pads. Here, the SI-InP substrate serves as a supporting structure for the diode [8].

Figure1 (b) illustrates the equivalent circuit model of the SBD, which is the basis of our extraction method. The Schottky junction is modeled as voltage-dependent junction capacitance (C_j) and resistance (R_j) [9]. R_s is the series resistance. The fringing field between both pads is modeled as a pad-to-pad capacitance (C_{pp}). The finger-to-pad coupling is modeled as C_{fp} and the self-inductance of the air-bridge finger is modeled as L_f [10].

Although the equivalent circuit is very mature and has been used for years, but a self-consistent method to find the accurate values of these parameters is still lacking. Here, we use the on-wafer measured S-parameter under different bias condition up to 40 GHz and an auxiliary de-embedding structure to find the accurate values. Then we compare the extracted values with the theoretical values, which are deduced from the DC-IV curve of SBD.

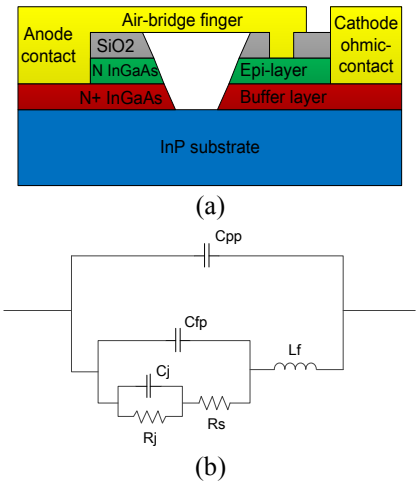

Fig. 1. (a) Cross section view and (b) equivalent circuit model of the InP/InGaAs based planar SBD.

Figure 2 shows the images of the diode which is identical to the one used in the detector and its auxiliary de-embedding structure. They are both in coplanar waveguide (CPW) configuration, since the ground-signal-ground (GSG) probe is used in the on-wafer S-parameter measurement.

In the extraction process, three equivalent circuits are used, which are "open", "short" and "actual", as shown in Fig. 3. "Open" represents the auxiliary de-embedding structure as shown in Fig. 2 (b). "Short" represents the SBD which is working at relatively large forward bias conditions, such as 1V. "Actual" represents the SBD which is working at bias conditions ranging from -1 V to 0.15 V. Notice that in all the three equivalent circuits, there should be a series resistance (denoted by R_{pad}) which represents the probe connection resistance and the resistance of the microstrip line. R_{pad} is removed from the circuits since it is very small (less than 1 Ω). The coupling between the signal and ground lines is modeled as C_{pad}. The self-inductance of the signal line is modeled as L_{pad}. For planar diodes, L_f is in the range of several to tens pico-henrys, whereas the capacitances are in the range of a tenth to tens of a femto-farad. At the measured frequencies, capacitances are dominant, compared to the inductance. Thus, L_f is negligible in the equivalent circuit. In the "short" mode, C_j is extremely small and R_s is negligible, compared to L_{pad}. And in "actual" mode, R_s is negligible small in comparison with the junction resistance.

In "open" mode, C_{pad} is extracted by using:

$$C_{pad} = \frac{\mathrm{Im}(Y_{11\_open})}{\omega}. \quad (1)$$

In "short" mode, L_{pad} is extracted by using:

$$L_{pad} = \frac{1}{\omega} \cdot \frac{1}{\mathrm{Im}(Y_{11\_open} - Y_{11\_short})}. \quad (2)$$

In "actual" mode, the total capacitance (C_{pp}+C_{fp}+C_j) is extracted by using:

$$C_{total} = \frac{1}{\omega} \cdot \frac{1}{\frac{1}{\mathrm{Im}(Y_{11\_actual} - Y_{11\_open})} + \frac{1}{\mathrm{Im}(Y_{11\_open} - Y_{11\_short})}}, \quad (3)$$

where Y is the Y-parameter calculated from the on-wafer measured S-parameter, and ω is the angular frequency.

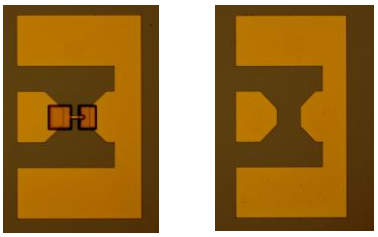

Fig. 2. Microscope images of: (a) diode and (b) auxiliary de-embedding structure in CPW configuration.

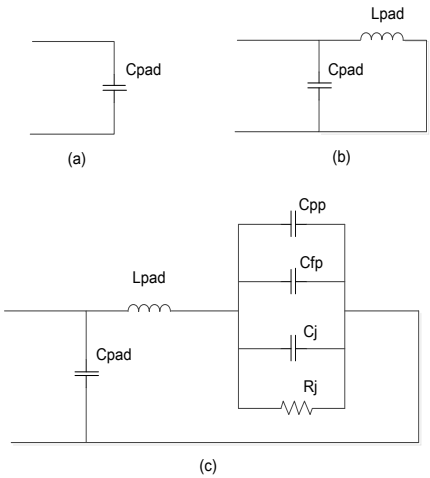

Fig. 3. Equivalent circuits for: (a) "open", (b) "short", and (c) "actual".

The measured S-parameter is from 10 to 40 GHz. Within this range, the extracted values of C_{pad}, L_{pad}, and C_{total} are about 19 fF, 95 pH and 18 fF, respectively, as shown in Fig. 4 (a), which is the case of the zero-bias condition. C_{pad} and L_{pad} do not change with different bias conditions, while C_{total} does; since it contains C_j, which is the voltage-dependent junction capacitance. The values of C_{total} under different bias conditions are shown in Fig. 4 (b), which is the case of 40 GHz.

According to the Schottky theory, the total capacitance is described as:

$$C_{total} = C_{j0}(1 - \frac{V}{V_{bi}})^{-0.5} + C_{par}, \quad (4)$$

where C_{j0} is the zero-bias junction capacitance, V is the bias voltage, V_{bi} is the build-in potential and C_{par} is the total parasitic capacitance (C_{pp} + C_{fp}).

By fitting (3) to (4), C_{j0}, V_{bi}, and C_{par} are extracted, which are useful in the design and simulation of the detector. From the curve-fitting procedure at 40GHz, C_{j0}, V_{bi}, and C_{par} are extracted as 9.6 fF, 0.26 V, and 8.8 fF, respectively. A comparison between the extracted and fitted C_{total} is depicted in Fig. 4 (b), showing a very good agreement. By using the same equation and values of C_{j0}, V_{bi}, and C_{par}, good agreements are also obtained at the band of 10-40 GHz.

The theoretical values of C_{j0} and V_{bi} are deduced from the DC-IV curve as 9.56 fF and 0.25 V respectively, which are consistent with the extracted values. Details of the deduction can be found in [6]. The values of these parameters are listed in Table 1.

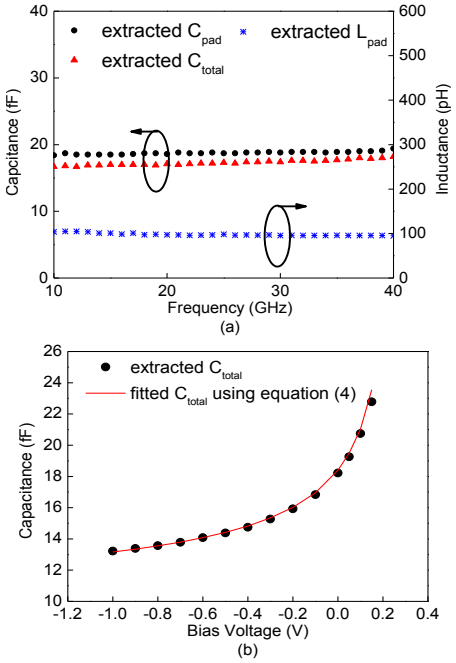

Fig. 4. (a) Extracted C_{total}, C_{pad}, and L_{pad} versus frequency at zero-biased voltage, and (b) extracted and fitted C_{total} versus bias voltage at 40 GHz.

Table 1: Summary of the values of parameters

Parameter	DC-IV Theory Value	Extracted Value (40 GHz)	Effective Value (400 GHz)
C_{j0}	9.56 fF	9.6 fF	$C_{j0,eft}$=15.7 fF
V_{bi}	0.25 V	0.26 V	$V_{bi,eft}$=0.26 V
C_{par}	-	8.8 fF	$V_{bi,eft}$=0.26 V
C_{pad}	-	19 fF	
L_{pad}	-	95 pH	

To verify our extraction method further, S-parameter comparison between equivalent circuit model simulation and diode measurement is presented. Figure 5 shows the simulated equivalent circuit as well as the value of each parameter which is obtained by our extraction method. The values of R_j is calculated by the DC-IV curve using:

$$R_j = \frac{dV}{dI} = \frac{1}{I} \cdot \frac{\eta kT}{q}, \tag{5}$$

where η is the ideal factor, q is the elementary charge, k is the Boltzmann's constant and T is the ambient temperature. The comparison between the simulated and measured S11 is shown in Fig. 6. Good agreements of both magnitude and phase are observed. Only S11 is compared here since the one-port measurement setup is used.

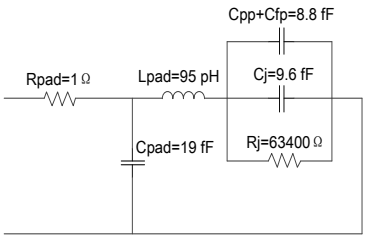

Fig. 5. Equivalent circuit simulation model with the values extracted by the proposed method.

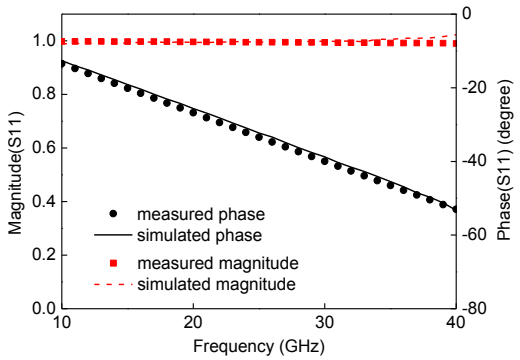

Fig. 6. Comparison between the simulated and measured S11 of the SBD.

The results in Fig. 4, Table 1 and Fig. 6 indicate that our method aiming at finding the accurate values of the parameters is valid, self-consistent and useful. The accurate values not only help us to get a deep insight of the diode which can help us to improve the diode, but also are the key to the diode modeling which is very important in the following detector design process.

However, the diode is expected to be used in a 340-400 GHz detector, which is beyond the extraction range (10-40 GHz). To solve this problem, an extrapolation process is conducted up to 400 GHz, as shown in Fig. 7. Only C_{total} is extrapolated since C_{pad} and L_{pad} are used to model the GSG configuration which has nothing to do with the modeling of the detector. It is observed that C_{total} varies with the frequency. The reason is that the parasitic effect becomes stronger at higher frequencies, which makes the circuit model in Fig. 1 (b) and Fig. 3 insufficient. However, fully considering the parasitic effect at high frequencies leads to a very complex question.

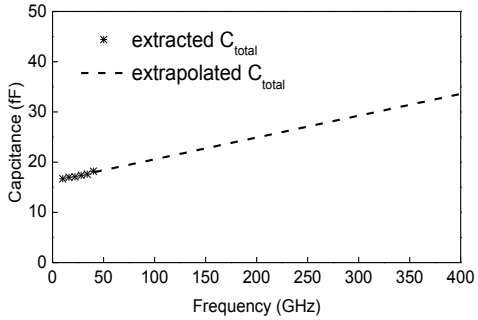

Fig. 7. Extracted and extrapolated C_{total} versus frequency at zero-biased voltage (markers are the extracted data calculated from the 10-40 GHz measured S-parameter, and dashed lines are the corresponding extrapolation up to 400 GHz).

So we proposed a concept called effective capacitance, which contains the high frequency parasitic effect while maintaining the same simplicity. In Section IV, we will see that the effective capacitance has greatly improved the consistency between the simulated and measured results of the detector. Figure 7 is the case of zero-biased condition. Extrapolation at other biased-conditions can be conducted in a similar way. Then a fitting procedure, which is similar to that in Fig. 4 (b) is conducted to obtain the effective C_{j0}, V_{bi} and C_{par} under 400 GHz, noted as $C_{j0,eft}$, $V_{bi,eft}$ and $C_{par,eft}$, respectively. All the values of the parameters are summarized in Table 1. It is observed that V_{bi} keeps the same value at DC, 40 GHz and 400 GHz, which is consistent with the physical properties of the material. $C_{j0,eff}$ and $C_{par,eff}$ are different from C_{j0} and C_{par}, since they now contain the high frequency parasitic effect.

In conclusion, the procedure of our modeling technology is as follows. Firstly, the extracted values at 10-40 GHz are obtained by using the proposed parameter extraction method. Then, an extrapolation process up to the operation frequency (400 GHz) is conducted to obtain the effective capacitance, which contains the high frequency effect and are used in the final circuit simulation. There are many other modeling technologies for SBD. For example, the model of drift-diffusion [11], hydrodynamic [12], and Monte Carlo [13] contains some physical effects, all of which could increase the accuracy, but are very complex and hard to implement with the conventional CAD tools. Other equivalent circuit models are always based on an I-V or C-V fitting procedure at low frequencies [14], which have too little physical insight.

And the lack of the extrapolation process makes the model inaccurate at high frequencies.

III. DESIGN OF THE DETECTOR

Generally, the detector can be divided into two parts, the linear part and the nonlinear part, which are analyzed by Ansoft's High Frequency Structure Simulator (HFSS) and Agilent's Advanced Design System (ADS), respectively. The proposed detector consists of four parts: waveguide (WG) to microstrip line transition, input matching, diode part, and output matching with low pass filter (LPF). The design process is shown in Fig. 8. Details of the design process are discussed as follows.

A 3D electromagnetic (EM) simulation model of the diode part including the connection to microtrip line is built in HFSS, as depicted in Fig. 9. This model is based on accurate geometric dimensions with the setup shown in Table 2. The definition of wave port representing the entrance to the Schottky junction is very important to achieve a correct simulation, which is defined as a circular sheet between the epi-layer and buffer layer with a perfect cylindrical conductor through the epi-layer.

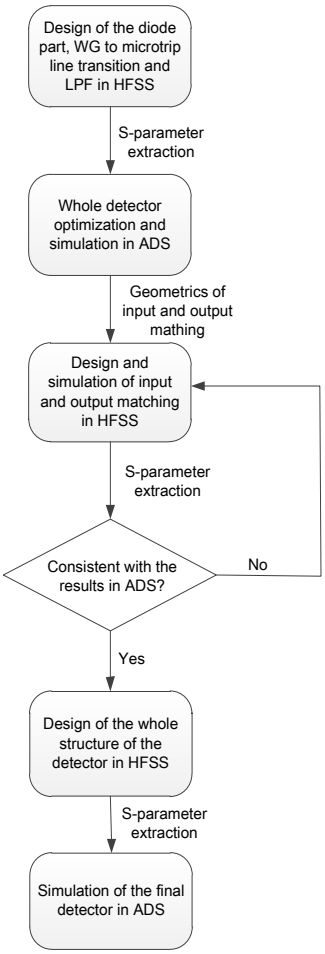

Fig. 8. Design flow of the detector.

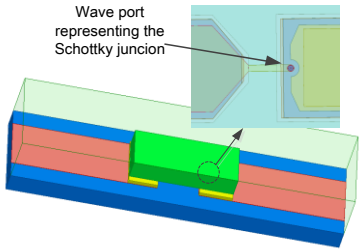

Fig. 9. 3D EM simulation model of the diode part and the definition of the wave port.

Table 2: Material properties setup in HFSS

Material	Relative Permittivity	Bulk Conductivity (S/m)
n^+ InGaAs	-	PEC
n InGaAs	12.3	0
SiO_2	4	0
InP	12.5	0

The passive linear parts of detector are designed and analyzed in HFSS and the nonlinear simulation is carried on in ADS by harmonic balance (HB) method. The circuit design process is introduced as follows. First, a WG to microstrip line transition and a LPF which stops the RF signal from leaking into the output port are designed. With the S-parameter data of the two structures, an ideal whole detector circuit model is built in ADS. After the optimization process, the initial structures of the input and output matching parts are obtained, which are then re-built in HFSS to verify the simulated results for the operating frequency is very high (340-400 GHz). The models in HFSS are modified to obtain the simulated results which are similar to those in ADS. Finally, the whole detector is built in HFSS, as depicted in Fig. 10, and simulated in ADS. A photograph of the detector is shown in Fig. 11.

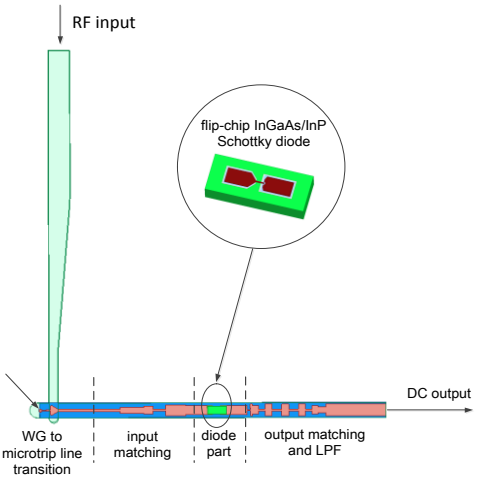

Fig. 10. Whole structure of the detector.

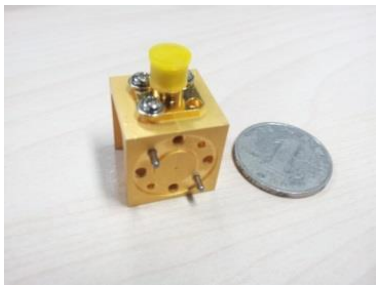

Fig. 11. Photograph of the detector.

IV. RESULTS

Voltage responsivity and NEP are two important characters of detectors. Voltage responsivity is defined as:

$$R_v = \frac{mag(V_{out})}{P_{in}}, \tag{6}$$

where V_{out} is the output voltage and P_{in} in the power of the pumped signal. The terahertz signal is pumped into the detector and then the output voltage is measured by a phase-locked amplifier. A comparison between the simulated and measured voltage responsivity of the detector is shown in Fig. 12. It is observed that the maximum measured voltage responsivity is 800 mV/mW at 382 GHz. Two different values of C_{j0} are used in the simulation. One is deduced from the DC-IV theory or extracted at 40 GHz, and the other is the effective value at 400 GHz using the concept of effective capacitance (see Table 1). Both the simulated results show the same trend of the measured result. However, a much better agreement is observed when using the effective capacitance at 400 GHz, which proves that our parameter extraction method, the corresponding extrapolation process and the concept of effective capacitance are valid and correct. Frankly speaking, there still exists some deviation, which may be due to the processing and assembling errors or even still the modeling technology. Although the deviation problem at high frequencies has not yet been completely solved, the proposed concept of effective capacitance is a very promising attempt.

NEP is defined as:

$$NEP = \frac{N_v}{R_v}, \tag{7}$$

where N_v is the noise voltage of detector, which is measured by noise analyzer. Commonly N_v is measured with zero RF power. Under this condition only thermal noise is generated, which is different from the actual condition. In fact, as the input power increases, excess noise such as flicker noise, is generated. Flicker noise becomes increasingly important as the input power is increased [15]. N_v is measured as 27.7×10^{-9} V/Hz$^{0.5}$ with a RF power level of about 4 μW, and then NEP is calculated, as shown in Fig. 13. The minimum NEP is 3.46×10^{-11} W/Hz$^{0.5}$ at 382 GHz.

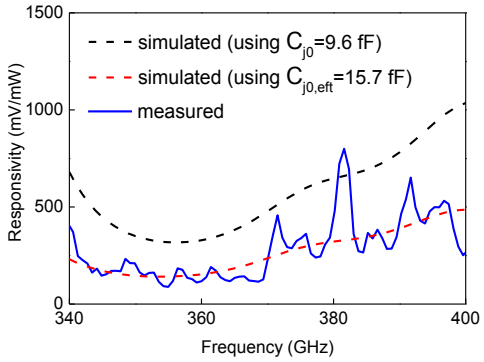

Fig. 12. Comparison between the measured and simulated voltage responsivity.

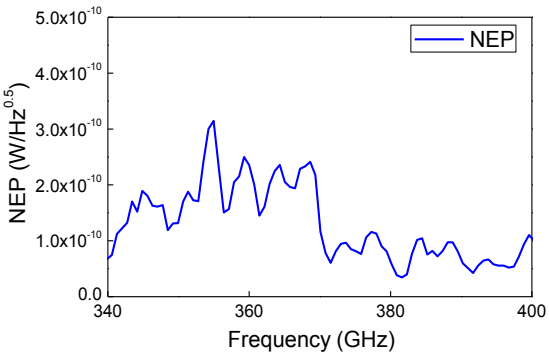

Fig. 13. Measured NEP of the detector.

V. CONCLUSION

In this study, firstly, we design and fabricate a type of InGaAs/InP material system based planar SBD with the feature of low barrier height which can improve the performance of detectors.

Secondly, a modeling technology for SBD is presented, which is based on an analytical parameter extraction method (working at 10-40 GHz) and a corresponding extrapolation process up to 400 GHz. The concept of effective capacitance is proposed to describe the high frequency effect, which greatly improve the consistency between the simulated and measured results of the detector.

Finally, based on the proposed SBD and the modeling technology, a 340-400 GHz zero-biased waveguide detector is designed and measured. By utilizing the topology of zero-bias (no DC path), the proposed detector becomes simple, compact and low cost. The measured results show that the maximum voltage responsivity and the minimum NEP are 800 mV/mW and 3.46×10^{-11} W/Hz$^{0.5}$ at 382 GHz, respectively. The consistency between the simulated and measured results of the detector has been greatly improved with the help of the effective capacitance.

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