A Three-Conductor Transmission Line Model for MOS Transistors

F. Daneshmandian, A. Abdipour, and R. Mirzavand

Electrical Engineering Department, Institute of Communications Technology and Applied Electromagnetics
Micro/mm-wave & Wireless Comm. Research Lab, Amirkabir University of Technology, Tehran, 15914, Iran
f.daneshmandian@yahoo.com, abdipour@aut.ac.ir, rmirzavand@aut.ac.ir

Abstract ─ An accurate high frequency small signal model for MOS transistors is presented. In the proposed model, by considering the layout of the MOS transistor, it is considered as a three-conductor transmission line. Then, a set of current-voltage equations are derived for the structure using the transmission line theory. These coupled equations are solved by the Finite-Difference Time-Domain (FDTD) technique in a marching-in-time process. To verify the model, the scattering parameters of a 0.13 μm transistor are extracted from the time domain results over the 1–100 GHz frequency band and compared with the results obtained from the available models and commercial simulator. The suggested model can be useful in design of various types of high frequency integrated circuits.

Index Terms ─ CMOS technology, distributed analysis, FDTD method, MOSFET model, transmission line model.

I. INTRODUCTION

The increasing demand of implementing low cost monolithic microwave integrated circuits leads to significant advancement in CMOS technology [1,2]. On the other hand, by increasing the operating frequencies, the modeling issue in such high-density integrated circuits becomes more imperative. For accurate device modeling an electromagnetic interaction must be taken into account, especially when the device dimension is on the order of the wavelength [3]. In such cases, distributed modeling approach can be used to consider the wave propagation effect along the MOS transistors. Distributed analysis method is based on the transmission line model of the transistors.

Distributed modeling of field effect transistors in the case of GaAs MESFET was previously studied [4,5]. In these studies the transistor is considered as a multi-conductor active transmission line. Also, transmission line modeling of transistor in the case of MOS transistor was formerly investigated [6-9], but in all these reports only the distributed effect of gate electrode of the MOS transistor are considered. In this paper, the approach used for MESFET transistor modeling is utilized for distributed modeling of MOS transistor based on three coupled transmission lines in CMOS technology, so the more accurate model for MOSFETs are achieved compared to the earlier models. In this approach, the transistor width is divided into a discrete number of segments and then by considering the proper equivalent circuit for each segment, the required equations for analysis of the transistor can be obtained. In other words, the transmission line theory is applied to each segment of transistor to obtain the wave equations in the MOS transistor structure [10-12]. To solve the attained system of active multi-conductor transmission line differential equations, a suitable method must be chosen. Since the time domain analytical solution doesn't exist for these equations, the finite-difference time-domain (FDTD) method, as a powerful and versatile numerical method is utilized for solving them [13-15]. The parasitic capacitances and inductances of the MOSFET model are numerically computed by solving the two-dimensional electrostatic field problem in the cross section of each transmission lines. By considering the layout of Fig. 1 and proposing that three electrodes of the transistor are placed on the 600 um silicon substrate, per unit-length capacitances and inductances in the MOSFET model are achieved by using finite difference method. Using these values in distributed model, results of proposed approach, Cadence SpectreRF simulator, lumped model, and an analytical approach which is based on the gate electrode distribution [9] are compared. It is shown that at low frequencies, the results of various models are the same while at higher frequencies, difference between them increases. It is expected that the distributed analysis describes the MOSFET behavior more accurate because of considering the wave propagation.

II. DISTRIBUTED SMALL SIGNAL FOR MOSFETS

The width of a MOSFET becomes in the order of wavelength at high frequencies and wave propagation along its electrodes must be considered. To investigate this distributed effect, a MOS transistor can be modeled as three coupled transmission lines on a silicon

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substrate while assuming the magnitude of longitudinal electromagnetic field is negligible with respect to the transverse one. Therefore, the device electrodes can be considered in just the dominant quasi-TEM mode. For numerical simulation, transistor's electrodes must be divided into some segments in propagation direction while considering active and passive equivalent circuit for each part, as shown in Fig. 2. The active part describes the small signal behavior of intrinsic device, and the passive part indicates electromagnetic interaction between electrodes. All parameters in the active and passive parts are per unit-length values. In the limiting case of $\Delta z \to 0$, using Kirchhoff's circuit laws in the circuit of Fig. 2 for drain, gate, and source currents and voltages, i.e., I_d, V_d, I_g, V_g, and I_s, V_s, respectively, we have [4,5]:

$$\frac{\partial I_d}{\partial z}+\frac{\partial (C_1V_d-C_{12}V_g-C_{13}V_s)}{\partial t}+G_{ds}(V_d-V_s) +G_mV_g'=0, \tag{1}$$

$$\frac{\partial V_d}{\partial z}+R_dI_d+\frac{\partial (L_dV_d+M_{dg}V_g+M_{ds}V_s)}{\partial t}=0, \tag{2}$$

$$\frac{\partial I_g}{\partial z}+\frac{\partial (C_2V_g-C_{23}V_g+C_{gs}V_g'-C_{12}V_d)}{\partial t}=0, \tag{3}$$

$$\frac{\partial V_g}{\partial z}+R_gI_g+\frac{\partial (L_gV_d+M_{dg}V_g+M_{gs}V_s)}{\partial t}=0, \tag{4}$$

$$\frac{\partial I_s}{\partial z}+\frac{\partial (C_3V_s-C_{13}V_d-C_{23}V_g)}{\partial t}-C_{gs}V_g' -G_{ds}(V_d-V_s)-G_mV_g'=0, \tag{5}$$

$$\frac{\partial V_s}{\partial z}+R_sI_s+\frac{\partial (L_sV_d+M_{ds}V_g+M_{gs}V)}{\partial t}=0. \tag{6}$$

Using V_g' as the voltage on C_{gs}, another equation can be written as:

$$V_g'+V_s+R_iC_{gs}\frac{\partial V_g'}{\partial t}-V_g=0, \tag{7}$$

where

$$\begin{aligned} C_1&=C_{dp}+C_{ds}+C_{dsp}+C_{dg}+C_{dgp},\\ C_2&=C_{gp}+C_{gsp}+C_{dg}+C_{dgp},\\ C_3&=C_{sp}+C_{ds}+C_{dsp}+C_{gsp},\\ C_{12}&=C_{dg}+C_{dgp},C_{13}=C_{ds}+C_{dsp},C_{23}=C_{gsp}. \end{aligned} \tag{8}$$

Equations (1)-(6) can simplify to matrix form of:

$$\frac{\partial \mathbf{V}}{\partial z}+L\frac{\partial \mathbf{I}}{\partial t}+R\mathbf{I}=0, \tag{9}$$

$$\frac{\partial \mathbf{I}'}{\partial z}+C\frac{\partial \mathbf{V}'}{\partial t}+G\mathbf{V}'=0, \tag{10}$$

with the following definitions:

$$\begin{aligned} \mathbf{V}(z,t)&=\left[V_d,V_g,V_s\right]^T(z,t),\\ \mathbf{I}(z,t)&=\left[I_d,I_g,I_s\right]^T(z,t),\\ \mathbf{V}'(z,t)&=\left[V_d,V_g,V_s,V_g'\right]^T(z,t),\\ \mathbf{I}'(z,t)&=\left[I_d,I_g,I_s,0\right]^T(z,t), \end{aligned} \tag{11}$$

$$C=\begin{pmatrix} C_1 & -C_{12} & -C_{13} & 0\\ -C_{12} & C_2 & -C_{23} & C_{gs}\\ -C_{13} & -C_{23} & C_3 & -C_{gs}\\ 0 & 0 & 0 & R_iC_{gs}\end{pmatrix}, \tag{12}$$

$$G=\begin{pmatrix} G_{ds} & 0 & -G_{ds} & G_m\\ 0 & 0 & 0 & 0\\ -G_{ds} & 0 & G_{ds} & -G_m\\ G_m & -1 & -1 & 1\end{pmatrix},$$

$$L=\begin{pmatrix} L_d & M_{dg} & M_{ds}\\ M_{dg} & L_g & M_{ds}\\ M_{ds} & M_{gs} & L_s\end{pmatrix}, R=\begin{pmatrix} R_d & 0 & 0\\ 0 & R_g & 0\\ 0 & 0 & R_s\end{pmatrix}. \tag{13}$$

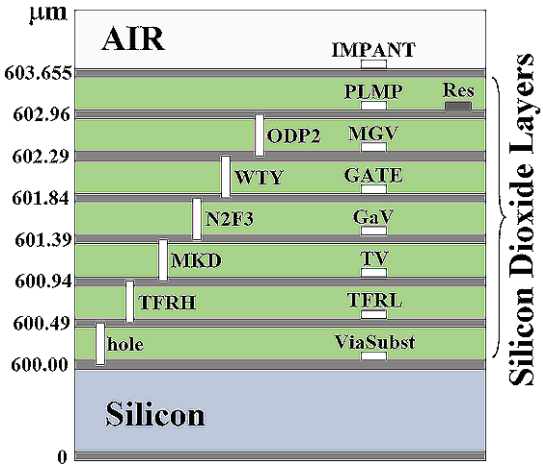


Fig. 1. The layout of a 130 nm CMOS technology.

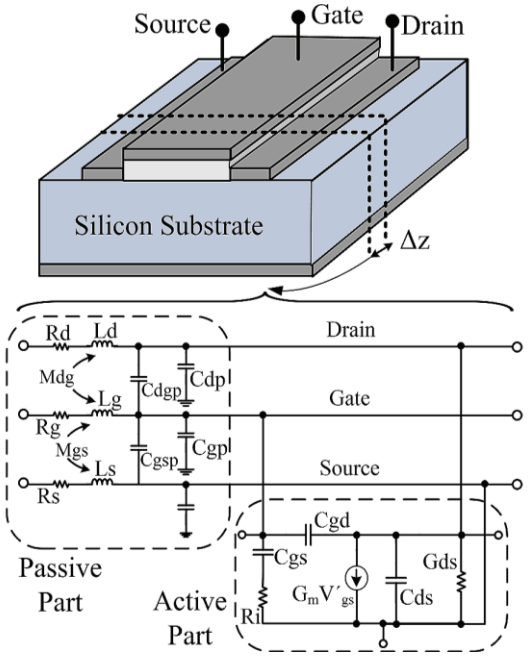


Fig. 2. A MOSFET and its partial equivalent model.

In order to apply the FDTD method to above equations of the MOSFET, total length and simulation time are divided into *Nz* and *Nt* sections with length of Δz and Δt, respectively. Adjacent voltage and current points are separated by half of Δz and half of Δt, as illustrated in Fig. 3. Then, applying FDTD to (9) and (10) leads to:

$$\frac{\mathbf{V}_{k+1}^{n+1}-\mathbf{V}_{k}^{n+1}}{\Delta z}+L\frac{\mathbf{I}_{k}^{n+3/2}-\mathbf{I}_{k}^{n+1/2}}{\Delta t} +R\frac{\mathbf{I}_{k}^{n+3/2}+\mathbf{I}_{k}^{n+1/2}}{2}=0, \tag{14}$$

$$\frac{\mathbf{I}_{k}^{\prime n+1/2}-\mathbf{I}_{k-1}^{\prime n+1/2}}{\Delta z}+C\frac{\mathbf{V}_{k}^{\prime n+1}-\mathbf{V}_{k}^{\prime n}}{\Delta t} +G\frac{\mathbf{V}_{k}^{\prime n+1}+\mathbf{V}_{k}^{\prime n}}{2}=0, \tag{15}$$

where

$$\begin{aligned}\mathbf{V}_{j}^{i}&=\mathbf{V}((i-1)\Delta z, j\Delta t),\\ \mathbf{V}_{j}^{\prime i}&=\mathbf{V}'((i-1)\Delta z, j\Delta t),\\ \mathbf{I}_{j}^{i}&=\mathbf{I}((i-1/2)\Delta z, j\Delta t),\\ \mathbf{I}_{j}^{\prime i}&=\mathbf{I}'((i-1/2)\Delta z, j\Delta t).\end{aligned} \tag{16}$$

Solving (14) and (15) gives the required recursion relations for computing voltages and currents in each interior point on the transistor electrodes as:

$$I_{k}^{\prime n+3/2}=\left(\frac{L}{\Delta t}+\frac{R}{2}\right)^{-1}\left\{\left(\frac{L}{\Delta t}-\frac{R}{2}\right)I_{k}^{\prime n+1/2} -\frac{V_{k+1}^{\prime n+1}-V_{k}^{\prime n+1}}{\Delta z}\right\};k=1,2,...,N_Z, \tag{17}$$

$$V_{k}^{\prime n+1}=\left(\frac{C}{\Delta t}+\frac{G}{2}\right)^{-1}\left\{\left(\frac{C}{\Delta t}-\frac{G}{2}\right)V_{k}^{\prime n} -\frac{I_{k}^{\prime n+1/2}-I_{k-1}^{\prime n+1/2}}{\Delta z}\right\};k=2,3,...,N_Z. \tag{18}$$

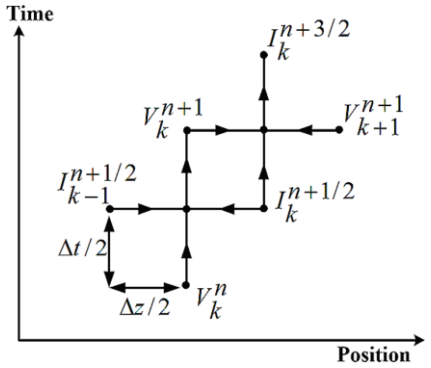


Fig. 3. The current and voltage solution points in space and time for the FDTD analysis.

Equations (18) and (17) are calculated in order with marching manner to obtain voltage and current along the electrodes. To find the boundary conditions, voltage and current at the beginning of transistor can be written using (18) and circuit of Fig. 4 (a) as:

$$V_{1}^{\prime n+1}=\left(\frac{C}{\Delta t}+\frac{G}{2}\right)^{-1} \cdot\left\{\left(\frac{C}{\Delta t}-\frac{G}{2}\right)V_{1}^{\prime n}-\frac{I_{1}^{\prime n+1/2}-I_{0}^{\prime n+1/2}}{\Delta z/2}\right\}, \tag{19}$$

$$I_{0}^{\prime}=\frac{V_{in}^{\prime n}+V_{in}^{\prime n+1}-V_{1}^{\prime n}-V_{1}^{\prime n+1}}{2R_S^{\prime}}, \tag{20}$$

$$V_{in}^{'}=\begin{pmatrix}V_{ind}\\ V_{ing}\\ V_{ins}\\ 0\end{pmatrix}, G_s^{'}=\frac{1}{R_s^{'}}\begin{pmatrix}G_{sd}&0&0&0\\ 0&G_{sg}&0&0\\ 0&0&G_{ss}&0\\ 0&0&0&0\end{pmatrix}. \tag{21}$$

Then, equations (19) and (20) give a boundary value as:

$$V_{1}^{\prime n+1}=\left(\frac{C}{\Delta t}+\frac{G}{2}+\frac{1}{R_S^{\prime}\Delta z}\right)^{-1} \cdot\left\{\begin{array}{l}\left(\frac{C}{\Delta t}-\frac{G}{2}-\frac{1}{R_S^{\prime}\Delta z}\right)V_{1}^{\prime n}\\ -\frac{2}{\Delta z}(I_{1}^{\prime n+1/2}-\frac{V_{in}^{\prime n}-V_{in}^{\prime n+1}}{2R_S^{\prime}})\end{array}\right\}. \tag{22}$$

Similarly, from (18) and Fig. 4 (b) we have:

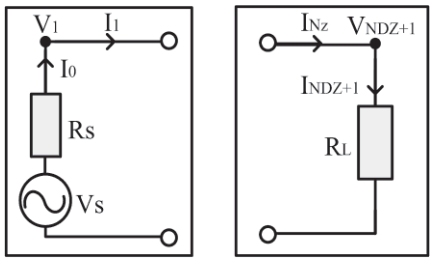
$$V_{Nz+1}^{\prime n+1}=\left(\frac{C}{\Delta t}+\frac{G}{2}\right)^{-1} \cdot\left\{\left(\frac{C}{\Delta t}-\frac{G}{2}\right)V_{Nz+1}^{\prime n}-\frac{I_{Nz+1}^{\prime n+1/2}-I_{Nz}^{\prime n+1/2}}{\Delta z/2}\right\}, \tag{23}$$

$$I_{Nz+1}^{\prime}=\frac{V_{Nz+1}^{\prime n}+V_{Nz+1}^{\prime n+1}}{2R_L^{\prime}}, \tag{24}$$

$$G_L^{'}=\frac{1}{R_L^{'}}\begin{pmatrix}G_{Ld}&0&0&0\\ 0&G_{Lg}&0&0\\ 0&0&G_{Ls}&0\\ 0&0&0&0\end{pmatrix}, \tag{25}$$

which give another boundary value as:

$$V_{Nz+1}^{\prime n+1}=\left(\frac{C}{\Delta t}+\frac{G}{2}+\frac{1}{R_L^{\prime}\Delta z}\right)^{-1} \left\{\left(\frac{C}{\Delta t}-\frac{G}{2}-\frac{1}{R_L^{\prime}\Delta z}\right)V_{Nz+1}^{\prime n}+\frac{2}{\Delta z}(I_{Nz}^{\prime n+1/2})\right\}. \tag{26}$$



(a) Source (b) Load

Fig. 4. Discretization at source and load terminals.

Now, we can start with an initially relaxed line having zero voltage and current values and find the voltages by equations (22), (18), and (26). It must be noted that to have a stable numerical solution, the space and time steps must satisfy the Courant condition [16]:

$$\Delta t \le \Delta z / v, \tag{27}$$

where v is the maximum velocity of wave propagation along the electrodes of transistor.

In this modeling approach the intrinsic parameters of MOS transistor including g_m, C_{gs}, C_{ds}, C_{gd}, R_i, and G_{ds} are computed based on the accurate physical based model of the MOSFET, BSIM3v3. In this model, the drain-source current in all regions is expressed as follows:

$$I_{ds} = \frac{I_{ds0}(V_{dseff})}{1+\frac{R_{ds} I_{ds0}(V_{dseff})}{V_{dseff}}}(1+\frac{V_{ds}-V_{dseff}}{V_A}) \cdot(1+\frac{V_{ds}-V_{dseff}}{V_{ASCBE}}). \tag{28}$$

By using the drain-source current, the transistor conductance G_m can be obtained as:

$$G_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}=Const.} \tag{29}$$

Also, all capacitances are derived from the charges to ensure charge conservation as:

$$C_{ij} = \frac{\partial Q_i}{\partial V_j}; \; i,j = g,d,s,b, \tag{30}$$

where the terminal charges Q_g, Q_b, Q_s, and Q_d are the charges associated with the gate, bulk, source, and drain terminals, respectively. The details of this model containing other equations and the parameters description are given in [17].

III. RESULTS AND DISCUSSION

In order to analyze the MOS transistor based on the discussed approach, a one finger MOSFET with gate dimension of 0.13×10 μm is proposed. A schematic of the proposed transistor and its relevant boundary condition is shown in Fig. 5. As shown, the beginning of gate electrode is connected to the source voltage V_S and resistance R_S, and the end of drain electrode is connected to a load R_L. In this example, both R_S and R_L are considered to be 50 ohm. Furthermore, the end of gate electrode and the beginning of drain electrode are open, while both sides of the source electrode are grounded.

The per-unit-length parameters of the intrinsic MOSFET are obtained at the V_{gs}=1.2 V and V_{ds}=1.2 V bias point, using the BSIM3v3 model and applying scaling technique. The per-unit-length capacitance and inductance matrixes of the passive part of the transistor are numerically determined by solving the two-dimensional electrostatic field problem in the cross section of each transmission lines based on the layout of Fig. 1. The per-unit-length resistances of the passive part of the MOSFET are achieved by considering the skin effect of the transistor electrodes [18]. The achieved parameters are listed in Table 1. The transistor is simulated by applying a small signal input voltage with amplitude of 0.05 V to achieve the voltages and currents of all points of the electrodes at different frequencies.

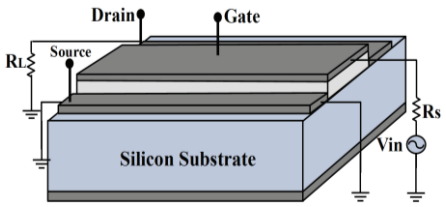


Fig. 5. Schematic of simulated MOSFET.

Table 1: The per-unit-length parameters of the passive part in the distributed MOSFET model

Element	The Per-Unit-Length Values
L_d	1.919 μH/m
L_s	1.919 μH/m
L_g	1.95 μH/m
M_{gd}	1.54 μH/m
M_{gs}	1.54 μH/m
M_{ds}	1.407 μH/m
R_d	600 kΩ/m
R_s	600 kΩ/m
R_g	740 kΩ/m
C_{gp}	136.75 pF/m
C_{dp}	110.5 pF/m
C_{sp}	110.5 pF/m
C_{gdp}	63.07 pF/m
C_{gsp}	63.07 pF/m
C_{dsp}	29.65 pF/m

The scattering parameters of the transistor are extracted from the time domain results at 1-100 GHz frequency band and compared with those of obtained by the analytical approach based on gate electrode distribution in [9], lumped model of the MOS transistor, and also simulator. Figure 6 and Fig. 7 show the magnitude and the phase of scattering parameters of the transistor, respectively. It seems that the results of distributed analysis based on three-conductor, one-conductor and lumped models are in close agreement at low frequencies. But, by increasing the frequency, the difference between the results becomes larger. Especially at higher frequencies, the result of our distributed model is closer to the Cadence SpectreRF simulator result. Due to the fact that at high frequencies the transistor dimensions become comparable with the wavelength, difference between various modeling

approaches becomes more obvious. In such cases, the distributed analysis of the transistor based on three-conductor transmission line can describe the behavior of the device at high frequencies more accurate than others. As the further work, to achieve more precise results, one can develop the discussed approach based on the nonlinear model of an intrinsic MOSFET and also used this model for distributed analysis and design of integrated circuits, so a monolithic analysis of the circuit can be realized.

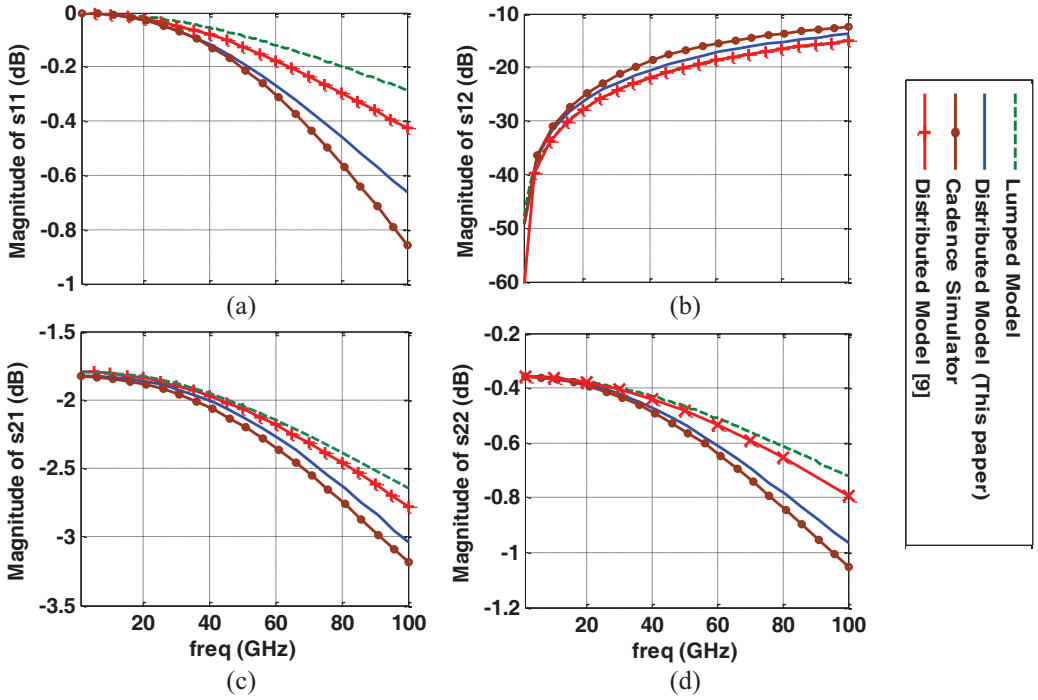


Fig. 6. The magnitude of scattering parameters of the MOS transistor: (a) S_{11}, (b) S_{12}, (c) S_{21}, and (d) S_{22}.

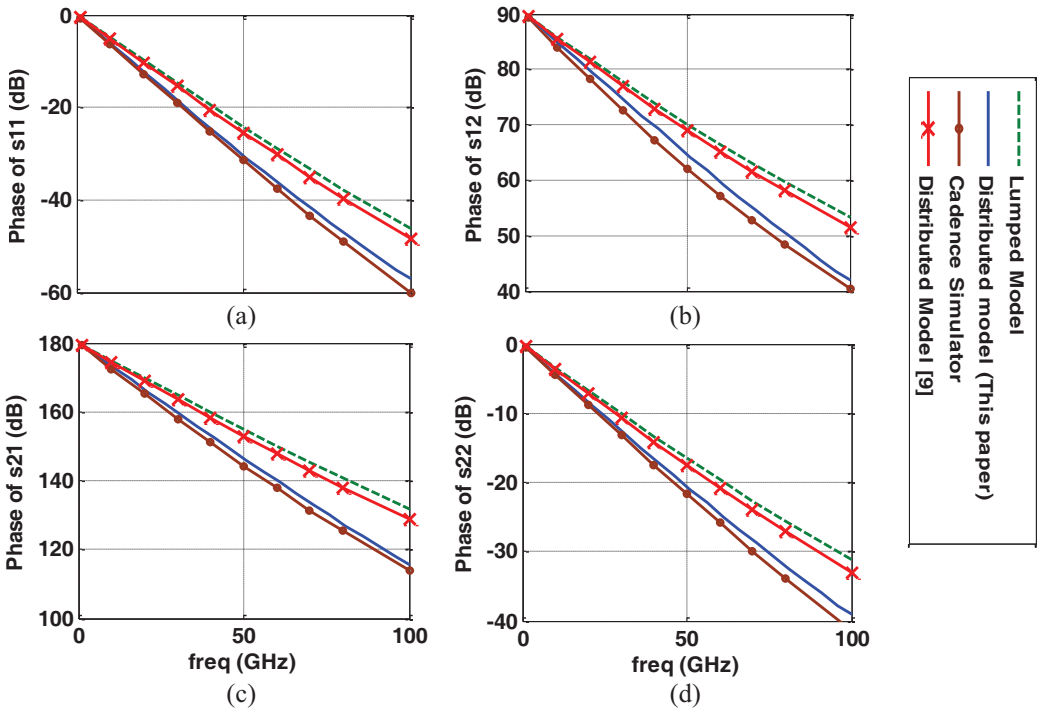


Fig. 7. The phase of scattering parameters of the MOS transistor: (a) S_{11}, (b) S_{12}, (c) S_{21}, and (d) S_{22}.

IV. CONCLUSION

A small signal model for high frequency MOSFETs based on three coupled transmission lines structure is investigated. The relevant differential equations of that structure are derived and solved using the FDTD method. By applying the proposed approach to a 0.13 μm MOS transistor, the small signal parameters are obtained from the time domain results at 1–100 GHz frequency band and compared with the conventional models. Results of the proposed distributed model show a close agreement with other models at low frequencies. But for the higher frequencies the differences become significant and the obtained result of proposed method is closer to the commercial simulator. Therefore, the three-conductor transmission line modeling of MOS transistors is more precise than other conventional approaches.

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Farzaneh Daneshmandian was born in Tehran, Iran, in 1989. She achieved her B.Sc. degree in Electrical Engineering in 2011 and M.Sc. degree in Communication in 2013 from Amirkabir University of Technology, Tehran, Iran. Her research areas include EM modeling of active devices and circuits, RF/ microwave and mm-wave MMIC circuit design, and nonlinear modeling of active devices. She is currently a Ph.D. student at Amirkabir University of Technology.

Abdolali Abdipour was born in Alashtar, Iran, in 1966. He received his B.Sc. degree in Electrical Engineering from Tehran University, Tehran, Iran, in 1989, his M.Sc. degree in Electronics from Limoges University, Limoges, France, in 1992, and his Ph.D. degree in Electronic Engineering from Paris XI University, Paris, France, in 1996. He is currently a Professor with the Electrical Engineering Department, Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran. He has authored four books in Persian and authored or co-authored over 300 papers in refereed journals and local and international conferences. His research areas include wireless communication systems, RF/ microwave/millimeter-wave circuit and system design, electromagnetic modeling of active devices and circuits, high-frequency electronics (signal and noise), and nonlinear modeling. Currently, he is Director of the Institute of Communications Tech. and Applied Electromagnetics, Amirkabir University of Technology, Tehran, Iran.

Rashid Mirzavand was born in Boroujen, Iran, in 1983. He received the B.Sc. degree from Isfahan University of Technology, Isfahan, Iran, in 2004, M.Sc. and Ph.D. degrees from Amirkabir University of Technology, Tehran, Iran, in 2007 and 2011, all in Electrical Engineering. In 2009, he joined the Centre for Analysis, Scientific Computing and Applications, Eindhoven University of Technology, Eindhoven, The Netherlands, as a visiting Ph.D. student. Since 2011, he's been a Research Assistant Professor with the Institute of Communications Tech. and Applied Electromagnetics, Amirkabir University of Technology, Tehran, Iran. He is the recipient of the Alberta Innovates Technology Futures (AITF) Post-Doctoral Fellowship and is currently a Research Associate with the Intelligent Wireless Technology Laboratory, University of Alberta, Edmonton, Canada. His research interests are in the areas of intelligent integrated sensors and antennas, microwave & mm-wave circuits and wireless systems, and computational electromagnetic.