# Design, Simulation and Fabrication of a Wide Bandwidth Envelope Tracking Power Amplifier

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***Abstract*** ─ In this paper an envelope tracking power amplifier is designed and implemented using MRF6S27015N MOTOROLA transistor in LDMOS technology. First, the amplifier is designed using load pull simulation and its parameters are optimized to increase the power added efficiency. Next, envelope detector and envelope amplifier are designed and simulated and finally ET is applied to the amplifier which results in more than 50% of PAE in a wide range of input power with bandwidth of 200 MHz. Envelope detector circuit is fabricated using schotkey diode and envelope amplifier is manufactured using a mosfet, an op amp, and a comparator.

***Index Terms*** ─ Envelope amplifier, envelope elimination and restoration, power amplifier.

## I. INTRODUCTION

Power amplifier is the most important part in a communication system because it uses the most amount of energy in the system. So, good efficiency of power amplifier can decrease amount of heat generated, and therefore boost performance of the total system. Back off may be used to maintain linearity of the power amplifier, but this may result in decreasing the efficiency. Some techniques are proposed to overcome this problem like LINC, $\Delta\Sigma$ modulation, Doherty, and EER Polar modulator. The first two techniques show high linearity with a moderate efficiency [1, 2] and the latter two techniques show high efficiency with a moderate linearity characteristic [3, 4]. However, applying the digital predistortion (DPD) technique to the latter two techniques can enhance the moderate linearity adequately. Envelope tracking power amplifiers are used to increase efficiency of the power amplifier [5-10]. ET uses a linear PA and a controlled supply voltage, which tracks the input envelope. When the supply voltage tracks the instantaneous envelope modulation signal, it is called Wide Bandwidth ET (WBET) [11]; when the supply voltage tracks the long-term average of the input envelope power, it is called Average ET (AET) [12]; when the supply voltage switches to different step levels according to the input envelope power, it is called Step ET (SET) [13]. EER (envelope elimination and restoration) uses a combination of a high efficiency switch-mode PA with an envelope re-modulation circuit [14]. To employ high efficiency operation of EER and at the same time reduce the strict necessities of bandwidth and time-alignment, the "hybrid" EER structure was proposed in [15]. Total system efficiency is determined by the product of the envelope amplifier efficiency and the RF transistor drain/collector efficiency. As a result, a high-efficiency envelope amplifier is vital for the EER/ET system. High efficiency envelope amplifier is usually realized by a DC/DC converter, where the switching frequency is required to be several times the signal bandwidth. For narrow bandwidth applications, most high efficiency switching mode DC/DC converters are realized by traditional delta modulation [16] or pulse width modulation (PWM) [17] modulators. Envelope amplifier block diagram is shown in Fig. 1, which consists of an OPAMP to realize the voltage source, and a MOSFET to realize the current source. This envelope amplifier consists of a voltage source and a current source. Although the current source has high efficiency, the voltage source has low efficiency. Therefore, we like to get most of the output current from the current source. To control the current of the voltage source, we use a hysteretic current feedback control to realize the soft power division between switch stage and linear stage amplification. The load voltage is controlled by the linear voltage source, and the load current is a mixture of the linear stage current and the switch stage current.

## II. ET AMPLIFIER DESIGN

### A. RF amplifier design

Si-LDMOS is a popular device choice for base-station high-power amplifiers, since LDMOS technology can provide reliable and cost effective solutions [18]. Envelope tracking techniques, in which a wideband envelope amplifier makes variable supply biasing to the RF stage, have established excellent performance using

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a variety of device technologies including Si LDMOS and GaN FETs [19]. Nonetheless, the RF PA should have suitable characteristics to be appropriate for the envelope tracking operation and achieve the optimal performance such as low deviation of the output capacitance, since a large variation of the voltage dependent output capacitance will corrupt the average efficiency as the optimum impedance matching for the output of the PA changes with the supply voltage [17]. Besides, extra nonlinearity like AM-PM distortion from the nonlinear capacitance and AM-AM distortion from the envelope amplifier, and memory effects due to the limited bandwidth of the RF PA and the envelope amplifier is produced by the dynamic supply biasing. However, digital pre-distortion (DPD) techniques may be used to correct the nonlinearity of the dynamically biased amplifier. In this paper, the amplifier is designed and implemented using the MRF6S27015N MOTOROLA transistor in LDMOS technology and is simulated using ADS2008 software where nonlinear analysis is performed using harmonic balance method [20]. The design of the amplifier is at the central frequency of 2.1 GHz and the bandwidth of the RF amplifier is 200 MHz, which is high with respect to the other works. The amplifier is biased in class AB. Output current diagrams of the transistor is used to choose appropriate Vgs, which can be selected between 2.3 volt and 3.8 volt to work in class AB and is optimized to increase the efficiency.

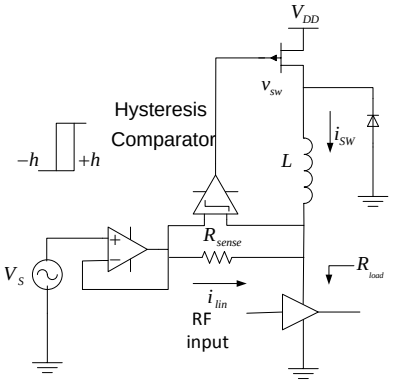


Fig. 1. Envelope amplifier block diagram.

Load pull simulation is used to select the optimum output impedance seen from the output of the transistor that increases the efficiency which is 5.7 + *j*12.6. Power added efficiency and gain of the transistor when it sees output impedance of 5.7 + *j*12.6, is shown in Fig. 2. Our aim in design of the power amplifier is to increase the efficiency. So, we optimized the amplifier to reach our goal and we changed Vgs, Vds, width and length of the matching transmission lines to reach to a good efficiency. Also, matching of the transistor is optimized in ADS software. Table 1 shows line width and line length of the optimized transmission lines. RO4003 substrate is used with $\varepsilon_r = 3.5$ and $\tan\delta = .0027$. Input matching and output matching schematics are shown in Fig. 3 and Fig. 4. Optimising the matching circuit in ADS software, input and output return losses are shown in Fig. 5 and Fig. 6.

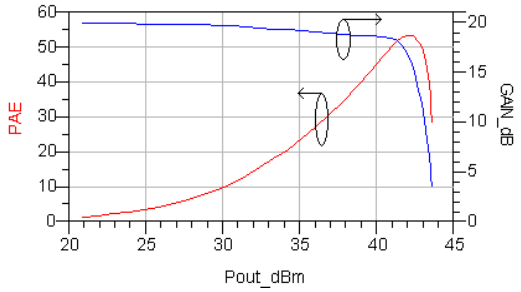


Fig. 2. Gain and power added efficiency versus output power for optimum output impedance.

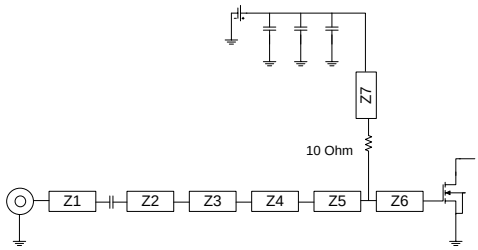


Fig. 3. Input matching circuit.

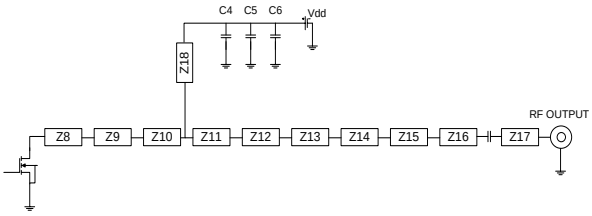


Fig. 4. Output matching circuit.

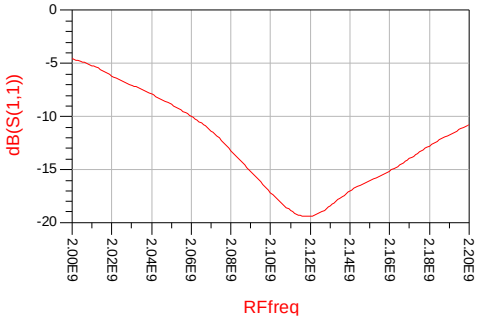


Fig. 5. Input matching

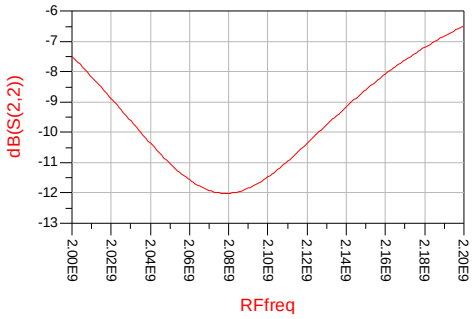


Fig. 6. Output matching.

Increasing the output power of the transistor will increase the PAE. However, our input signal has a high peak to average ratio and probability of the peak power is very low. Consequently, it is wise to design the matching for the case that happens most of the time, which is mean power. Therefore, because Vds changes with respect to the input power, we optimized the power amplifier for the Vds related to the mean power.

Table 1: Size of the matching transmission lines

| Line Number | Line Length (mil) | Line Width (mil) |
|---|---|---|
| Z1 | 940 | 25 |
| Z2 | 360 | 85 |
| Z3 | 170 | 145 |
| Z4 | 85 | 85 |
| Z5 | 370 | 800 |
| Z6 | 136 | 800 |
| Z7 | 800 | 20 |
| Z8 | 80 | 705 |
| Z9 | 100 | 900 |
| Z10 | 100 | 805 |
| Z11 | 200 | 805 |
| Z12 | 95 | 600 |
| Z13 | 80 | 405 |
| Z14 | 100 | 135 |
| Z15 | 705 | 40 |
| Z16 | 720 | 25 |
| Z17 | 100 | 44 |
| Z18 | 900 | 20 |

### B. Changing $V_{ds}$

In the next step, we changed Vds of the power amplifier from 8v up to 28v by 4v to show the possibility of increase in PAE by envelope tracking. Power added efficiency and output power of the RF power versus input power at center frequency of 2.1 GHz by changing Vds from 8v up to 28v by 4v is shown in Fig. 7 and Fig. 8 respectively. When the input power is 10 dBm and Vds is 8v, this simulation shows about 17% of more PAE than the condition of Vds=28v. Figure 7 shows that we can increase P1dB of the transistor when the input power is large by applying ET.

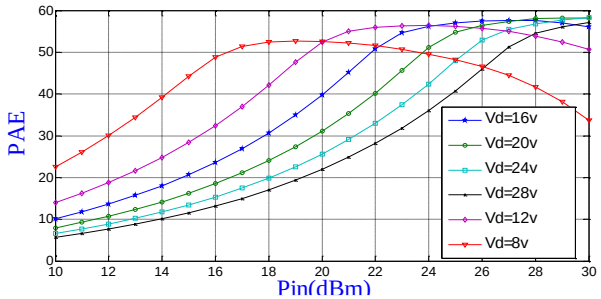


Fig. 7. PAE versus input power at center frequency by changing Vds.

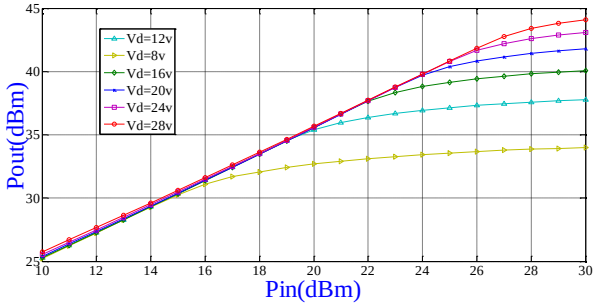


Fig. 8. Output power versus input power at center frequency by changing Vds.

### C. Applying ET

When Vds is 8v, the PAE decreases in the peak power, and when Vds is 28v the PAE is low in low power. To overcome this problem, we can apply envelope tracking to our amplifier. By changing the Vds with respect to the input power, we can see that the PAE remains above 50% for a wide range of input power. Figure 9 shows PAE versus input power at center frequency by applying envelope tracking respectively.

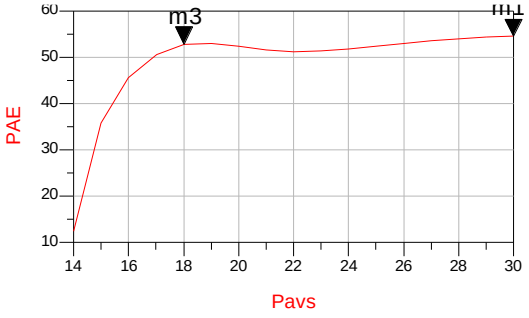


Fig. 9. PAE versus input power at center frequency by applying envelope tracking.

### D. Envelope detector

Envelope detector is shown in Fig. 10, which consists of a Schottky diode and an LC circuit by L=190 (nH) and C=18 (pF). HSMS286K Schottky diode produced by Agilent is used. Envelope detector is simulated in ADS software by the signal shown in Fig. 11 and the output signal is obtained.

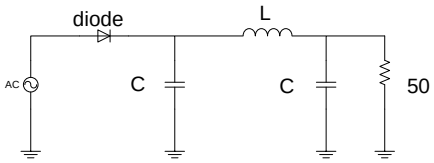


Fig. 10. Envelope detector.

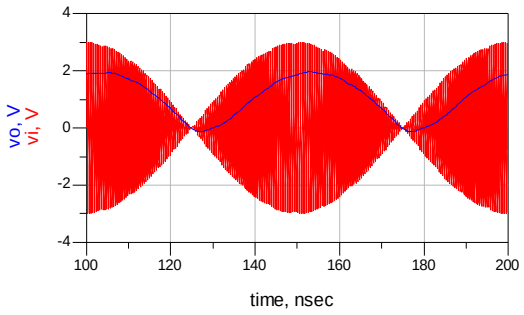


Fig. 11. Input and output signal of the envelope detector.

## III. FABRICATION AND TEST

Manufactured circuit is shown in Fig. 12 which consists of 3 parts: 1) Wilkinson power divider, 2) envelope detector, and 3) transistor. In part 1 a Wilkinson power divider is used to divide the input signal to two equal parts. One part is fed to the transistor and one part is fed to an envelope detector circuit.

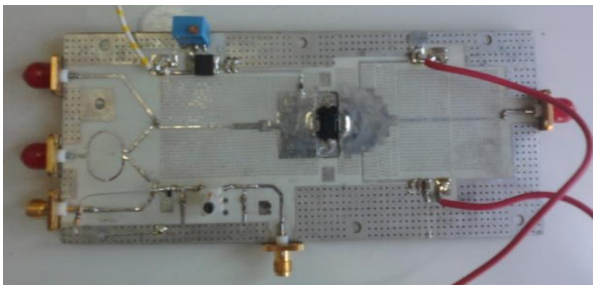

Fig. 12. Manufactured circuit.

Manufactured envelope amplifier circuit is shown in Fig. 13 and its block diagram is shown in Fig. 1, which consists of a mosfet, an op-amp, and a comparator where their part number is given in Table 2. Also, Table 3 compares previous works with this paper.

Gain versus input power at center frequency by changing Vds, output power versus input power at center frequency by changing Vds, and PAE versus input power at center frequency by changing Vds are shown in Fig. 14 up to Fig. 16.

Table 2: Envelope amplifier

| Device | Number | Producer |
|---|---|---|
| OP-AMP | THS3095 | TEXAS INSTRUMENT |
| MOSFET | FDFSP106A | FAIRCHILD |
| COMPARATOR | LM119J | NATIONAL |

Fig. 13. Manufactured envelope amplifier circuit.

Table 3: Comparison to previous envelope amplifiers

| | Power (dBm) | Envelope Amplifier BW (MHz) | Efficiency (%) |
|---|---|---|---|
| [4] | 29.7 | 10 | 82 |
| [5] | 23.2 | 20 | 65 |
| [6] | 28.9 | 10 | 76 |
| [7] | 27 | 10 | 71 |
| [8] | 30.8 | 4 | 75.5 |
| [9] | 33 | 4 | 89 |
| [10] | 28 | 1.25 | 82 |
| This work | 40 | 1 | 65 |

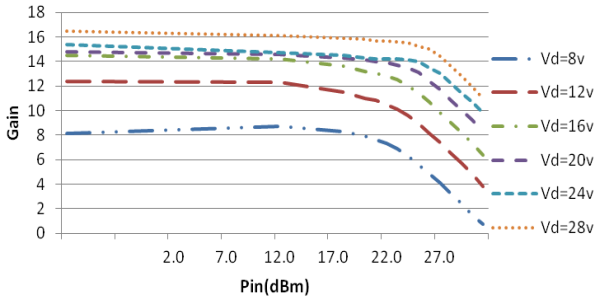


Fig. 14. Gain versus input power at center frequency by changing Vds.

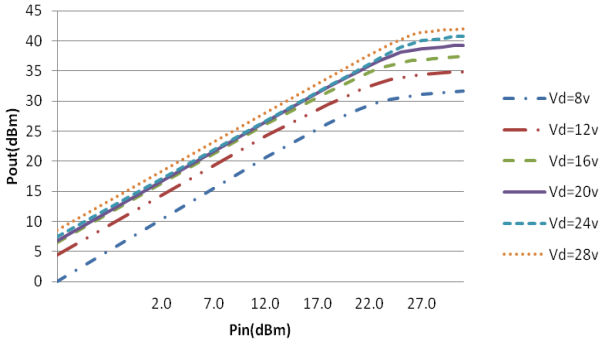


Fig. 15. Output power versus input power at center frequency by changing Vds.

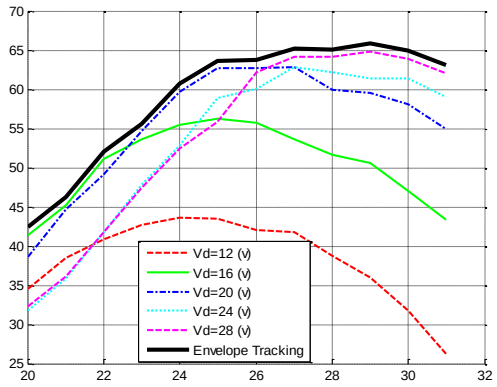


Fig. 16. PAE versus input power at center frequency by changing Vds.

## IV. CONCLUSION

In this research an ET amplifier in the frequency range of 2 GHz to 2.2 GHz has been designed and fabricated using MRF6S27015N MOTOROLA transistor in LDMOS technology which has 10 watts output power. Also, implementation of the envelope amplifier and envelope detector has been described. It has been shown that the PAE remains above 50% for a wide range of input power for a bandwidth of 200 MHz.

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