An Improved Design of Equal-Split Filtering Divider with Integrated Coupled-Line Band-Pass Filter

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Abstract ─ A novel methodology is proposed for achieving good output port isolation and return loss in a micro-strip filtering divider design with integrated coupled-line (CPL) band-pass filter (BPF). The designed filtering divider shows improved performance parameters as compared to previously reported work. It is proposed that by incorporating an extended transmission line (TL) and a conventional resistor as isolation elements, in addition to good even mode response (i.e., insertion loss IL, and input port return loss RL), the odd mode response (i.e., output port RL and isolation) can simultaneously be improved. In addition, two transmission zeros are realized in the vicinity of the pass band providing a reasonable skirt. Firstly, the coupled-line filter (CPLF) is matched to 70.7Ω and subsequently integrated in place of conventional quarter wavelength transformers in a Wilkinson Power Divider (WPD) for equal division. Under these matched conditions, it is shown that a TL section and isolation resistor sufficed to achieve a reasonable output port return loss (RL) and isolation in the resulting filtering divider. Experimental validation of the proposed methodology comes from the measurements results of the fabricated CPL filtering divider designed at 3 GHz conforming reasonably to the simulated ones. For instance, 1 dB fractional bandwidth of 15.3%, port isolation of better than 31 dB and good out-of-band performance up to $2.67f_0$ were experimentally achieved.

Index Terms ─ Band-pass filter, coupled line filter, equal split, filtering divider.

I. INTRODUCTION

Integration of band-pass filter (BPF) in a Wilkinson power divider (WPD) has drawn much research interest for realization of a filtering divider with low insertion loss (IL) and compact area as compared to when implemented separately in most RF front-ends (RFFE). The idea is to effectively replace the quarter wavelength transformers ($\lambda_g/4$, where λ_g is the guided wavelength) with a BPF (with certain fractional bandwidth (FBW)) in a power divider (PD) to improve the frequency selectivity, which is otherwise poor in a conventional WPD [1]. In addition, different isolation elements/techniques are employed between the output ports to achieve an acceptable port isolation and output return loss (RL). Many types of band pass filters have been used for the purpose for unequal/equal power division [2-8] with different isolation elements. For instance quasi-elliptical BPF was used in [2-3] with a single resistor as isolation element. In [2], a FBW of 4% was achieved with improved out of band rejection but output port isolation (using a resistor as isolation element) was only at 15 dB with high insertion loss of 6.4 dB. In [3], IL was improved to 3.99 dB with output port RL and isolation of 20 dB each, by employing a $\lambda_g/2$ resonator, four $\lambda_g/4$ resonators and an isolation resistor. The achieved FBW was 6.5% with a very high value of the isolation resistor (3.2 KΩ), deviating considerably from the conventional value of 100Ω. Coupled-line (CPL) structures and BPF have been extensively used to improve the frequency selectivity in WPD [4-8]. Unequal power division was addressed in [4-5]. For equal-split, a CPL structure with an isolation resistor was used in [6] to achieve a FBW of 16% but out-of-band response was not catered for and there were no transmission zeros. A coupled-line filter (CPLF) was used with a 3-dB hybrid as isolating element in [7]. Two prototypes were designed with port isolation of 24 dB. Here, although two transmission zeros were realized, but the IL was higher at 5.2 dB and 5.4 dB over a FBW 9.8% and 8.6% respectively. Moreover out-of-band rejection was less than $2f_0$ (where f_0 is the design frequency). A CPL section with defected ground structure (DGS) was used in [8] to achieve input port match and IL of 30 dB 3.15 dB respectively (even mode response). For effective output isolation, inductor, capacitor and resistor (LCR) were used and 23 dB of isolation and output port RL of 30 dB (odd mode response) was achieved. It may be noted here that third harmonic rejection was achieved with no transmission zeros. Two prototypes of filtering divider were presented in [9] by integrating second-order and fourth-order CPLF with a 3 dB FBW of 14.9% and 15.2% respectively. A port isolation of about 24 dB in both prototypes was achieved by employing a single resistor at the outputs. The IL however was high at 5.5 dB and 6.8 dB respectively. From the afore-said, there appears to be a tradeoff between the even mode response (Input

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port RL and IL) and odd mode response (output port RL and port isolation) of the filtering divider.

In this paper, a new methodology is presented which integrates a CPLF in WPD with an extended transmission line (TL) and resistor as isolation elements for improved performance parameters. It was previously established in our work [10-11] that a 50Ω extended TL section and a 100Ω resistor were sufficient to provide good isolation and output port RL in two and three TL dual band WPD. Here the concept is implemented on single-band filtering divider design to achieve simultaneous good even and odd mode response. A second order CPLF with a FBW of 16%, matched to 70.7Ω, has been shown to be effectively integrated in WPD maintaining low IL and good input matching as well as good output port matching and isolation. In addition, two transmission zeros are realized for a reasonably sharp skirt and good out-of-band rejection is achieved. For micro-strip implementation, using the proposed approach avoids usage of reactive elements. Moreover easily available SMD packages may be used to implement the conventional 100Ω resistor.

II. PROPOSED DESIGN DETAILS

A. Coupled-line filter (CPLF) design

Coupled lines/coupled line filters have been one of the famous choices for integration in the PD [4-9] as stated earlier. It is well established that even ordered filters are more appropriate to replace the conventional $\lambda_g/4$ transformers [4, 9]. In this subsection, design of a second order coupled line filter with Chebyshev response, pass-band ripple of 0.1 dB and FBW of 16% at a center frequency (CF) of 3 GHz is presented. Although design procedure of such CPLFs is well known [12], a brief design description is provided for brevity. For the laid down specification of the CPLF, firstly low pass filter prototype elements were calculated to be g_0=1, g_1=0.843, g_2=0.622 and g_3=1.355. By calculating the admittance (J) inverter values from Equations (1-3), band-pass conversion was carried out as a next step. Subsequently, form Equations (4-5), even and odd mode impedances were calculated. An important point to note here is that while designing the CPLF, the system impedance was taken to be 70.7Ω instead of 50Ω, in order to match the BPF in the PD circuit. This point is explained in detail in the next sub section.

With the values of impedances known and F4BM-2 taken as substrate with dielectric constant of 2.2 and height of 0.8 mm, widths (w) and distances (s) were calculated for each coupled line section as shown in Fig. 1 (a). Agilent's Advance Design System software (ADS) was used to carry out all simulations of the CPLF and CPLF divider. In order to get the desired response, the dimensions of the CPLF were slightly optimized and the final parameters are given in Table 1.

$$\frac{J_{01}}{Y_0} = \sqrt{\frac{\pi FBW}{2g_0 g_1}}, \tag{1}$$

$$\frac{J_{j,j+1}}{Y_0} = \frac{\pi FBW}{2}\frac{1}{\sqrt{g_j g_{j+1}}} \text{ (j = 1 to n-1)}, \tag{2}$$

$$\frac{J_{n,n+1}}{Y_0} = \sqrt{\frac{\pi FBW}{2g_n g_{n+1}}}, \tag{3}$$

$$(Z_{0e})_{j,j+1} = \frac{1}{Y_0}\left[1 + \frac{J_{j,j+1}}{Y_0} + \left(\frac{J_{j,j+1}}{Y_0}\right)^2\right], \tag{4}$$

$$(Z_{0o})_{j,j+1} = \frac{1}{Y_0}\left[1 - \frac{J_{j,j+1}}{Y_0} + \left(\frac{J_{j,j+1}}{Y_0}\right)^2\right] \text{ (j=0 to n).} \tag{5}$$

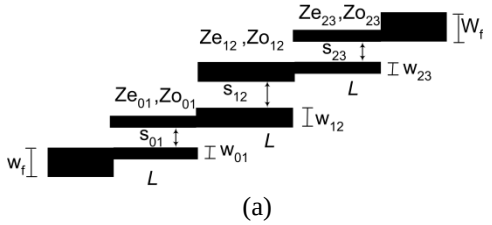
Where:

$J_{j,j+1}$ = Admittance (J) inverter parameters
Y_0 = Characteristic admittance of the terminating line (with Z0 = 70.7Ω)
FBW = Fractional Bandwidth = BW/centre frequency
N = Order of the filter
$(Z_{0e})_{j,j+1}$ = Even mode impedance
$(Z_{0o})_{j,j+1}$ = Odd mode impedance

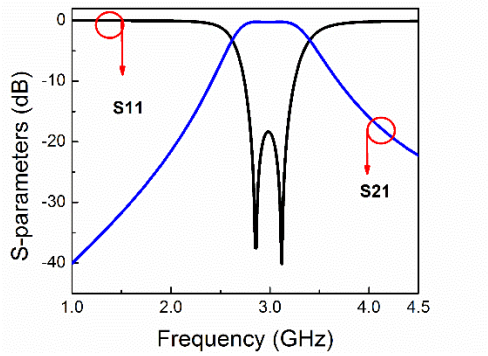
Table 1: Calculated design parameters of the CPLF

j	$J_{j,j+1}$	$(Z_{0e})_{j,j+1}$	$(Z_{0o})_{j,j+1}$	$w_{j,j+1}$ (mm)	$s_{j,j+1}$ (mm)
0	0.557	132.05	53.25	0.715	0.18
1	0.362	105.5	54.9	1.012	0.24
2	0.557	132.05	53.25	0.715	0.18

Please note that Z_0 was taken as 70.7Ω in the CPLF design equations for subsequent good match in the filtering divider. Simulation of the CPLF was carried out by setting the port impedance to 70.7Ω, due to which the width w_f of the feeding TLs at both connecting ends was taken equal to 1.386 mm (corresponding to 70.7Ω). Length L of each coupled line section was kept equal at $\lambda_g/4$ as shown in Fig. 1 (a). Figure 1 (b) depicts the simulated S-parameters response of the CPLF at 3 GHz with a 1 dB BW from 2.7 GHz to 3.2 GHz (FBW of 16.7%) achieving the desired specifications.



(a)



(b)

Fig. 1. (a) Second order coupled-line filter (CPLF) structure, and (b) simulated response of second order CPLF at 3 GHz.

B. Coupled-line filter divider (CPLFD) design

Proposed filtering divider circuit with a TL section and an isolation resistor is shown in Fig. 2 (a). The conventional $\lambda_g/4$ transformers have been replaced by second order CPLFs. A 50Ω extended TL section of length l_{TL} and a resistor R have been employed for effective output ports isolation and return loss (RL) [10, 11]. In order to get a simultaneous good even mode and odd mode response of the filtering PD, the TL length l_{TL} was optimized. Please note (refer to Fig. 3) that the outputs were tapped form zero position (the point where the BPFs end). Symmetry of the circuit in Fig. 2 (a) allows the even–odd mode analysis to be applied resulting in the half circuits as depicted in Figs. 2 (b) & (c) for even mode and odd mode respectively.

Under even mode excitations at the outputs, the proposed circuit can be bisected in the middle due to open circuit (magnetic wall) at the symmetric plane as shown in Fig. 2 (b). The isolation resistor R becomes superfluous and is shown as open circuit (OC). Assuming a system impedance of 50Ω, the input port 1 resistance doubles to a value of 100Ω in the bisected even mode circuit [1, 3]. Since the output port 2 is kept at 50Ω (system impedance), a transformation of 70.7Ω is required to achieve a perfect match between the input port and output port, as in conventional PD design [1]. In order to effectively replace the $\lambda_g/4$ transformer by a BPF, the latter must be matched to 70.7Ω so that Z_{in} = 50Ω as shown in Fig. 2 (b). This is exactly the reason that in the previous sub section, the port impedance was set to 70.7Ω instead of 50Ω for the CPLF simulation. Thus, under even mode condition, the proposed structure is expected to equally divide the signal with the filtering functionality as well, implying good IL and input port match (good RL).

Good output ports isolation and RL can be ensured through odd mode half circuit as shown in Fig. 2 (c) which results due to odd mode excitation at the output ports, forming a short circuit (electric wall) at the symmetric plane. Thus, port 1 is shorted and if port 2 is perfectly matched then, maximum power is delivered to the isolation resistor which is half of its original value and no (or very little) power is transferred to port 2 [1, 3]. Thus, for good isolation between the output ports 2 & 3 (each of 50Ω), the resistor value was taken to be 100Ω (R = 2 x 50 Ω). Best output port RL and isolation is achieved by optimizing l_{TL} of the TL which acts as an extension of the output port.

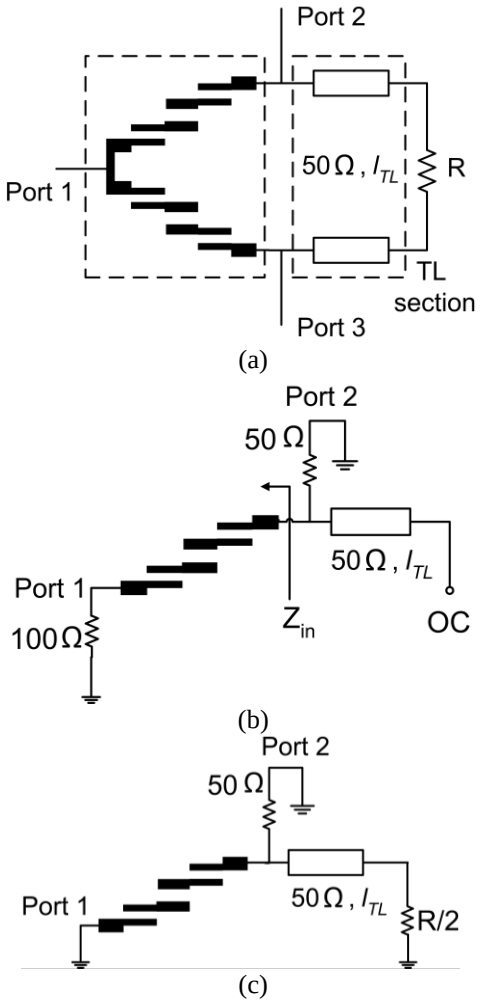


Fig. 2. (a) Proposed filtering divider, (b) even mode half circuit, and (c) odd mode half circuit.

It is imperative to mention here that the optimization of the TL length was carried out through the 'optimization tool' of the ADS in which the optimization goals were to achieve minimum value of S22/S33 and S23 by setting l_{TL} as variable (to be optimized in the range of $\lambda_g/8 < l_{TL} < \lambda_g/2$). This enabled accomplishing our purpose of attaining minimum S22/S33 and S23 just by optimizing the l_{TL} and keeping the R at a conventional value.

III. IMPLEMENTED FILTERING DIVIDER CIRCUIT

The designed filtering divider was fabricated on a F4BM-2 substrate with dielectric constant of 2.2 and height of 0.8 mm. Figure 3 shows the photo of the fabricated CPLFD. Please note that the TL length l_{TL} was optimized in the range of $\lambda_g/8 < l_{TL} < \lambda_g/2$ to get the best simultaneous even and odd mode response. Moreover, the output ports are shown to be tapped from zero position as marked in Fig. 3. Good functional response of the circuit was achieved at $l_{TL} = \lambda_g/2 = 37$ mm. The dimensions of the manufactured CPLFD are reported to be 10.1 cm × 2.4 cm (24.24 cm^2) or $1.3\lambda_g \times 0.3\lambda_g$. Although the size is slightly bigger in one dimension, but as will be shown in the results section, good simultaneous even and odd mode responses are achieved.

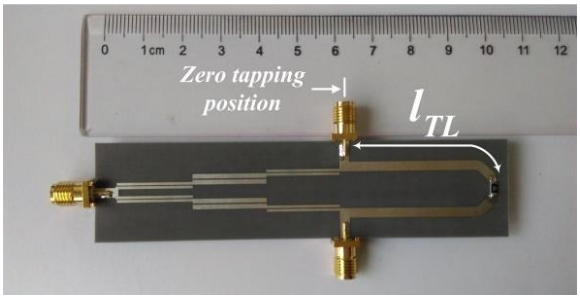


Fig. 3. Photograph of the manufactured CPLFD at 3 GHz.

IV. RESULTS AND DISCUSSION

All measurements of the fabricated CPLFD prototype were carried out on Agilent's PNA model no. E8363B. Figure 4 manifests the functional validity of the proposed technique which is evident through good conformance of measured and simulated S-parameter results at the design frequency of 3 GHz. Figure 4 (a) illustrates wide-band transmission response of the CPLFD with two transmission zeros at 1.4 GHz and 4 GHz. Moreover an out-of-band rejection of better than 15.8 dB was achieved up to $2.67f_0$ (8 GHz), since the first spurious pass-band appeared centered at about 8.5 GHz. Narrow band transmission characteristics are shown in Fig. 4 (b). Good symmetry of the designed circuit can be observed due to a fairly overlapping response of measured IL (S21 & S31). For even mode response, good input port match (S11) is reported to be at a measured value of 25 dB, while the insertion loss (S21 & S31) is at 3.45 dB (ideal value is 3 dB for equal division). Figures 4 (c) & (d) illustrate the odd mode response. From Fig. 4 (c), it is clear that the output port RL, (S22 and S33) stand at 29 dB each manifesting good match. Measured output port isolation (another very important performance parameter) is at 31 dB as shown in Fig. 4 (d). The designed CPLFD is operational over a measured 1 dB BW from 2.71 GHz to 3.17 GHz (1 dB FBW of 15.3%).

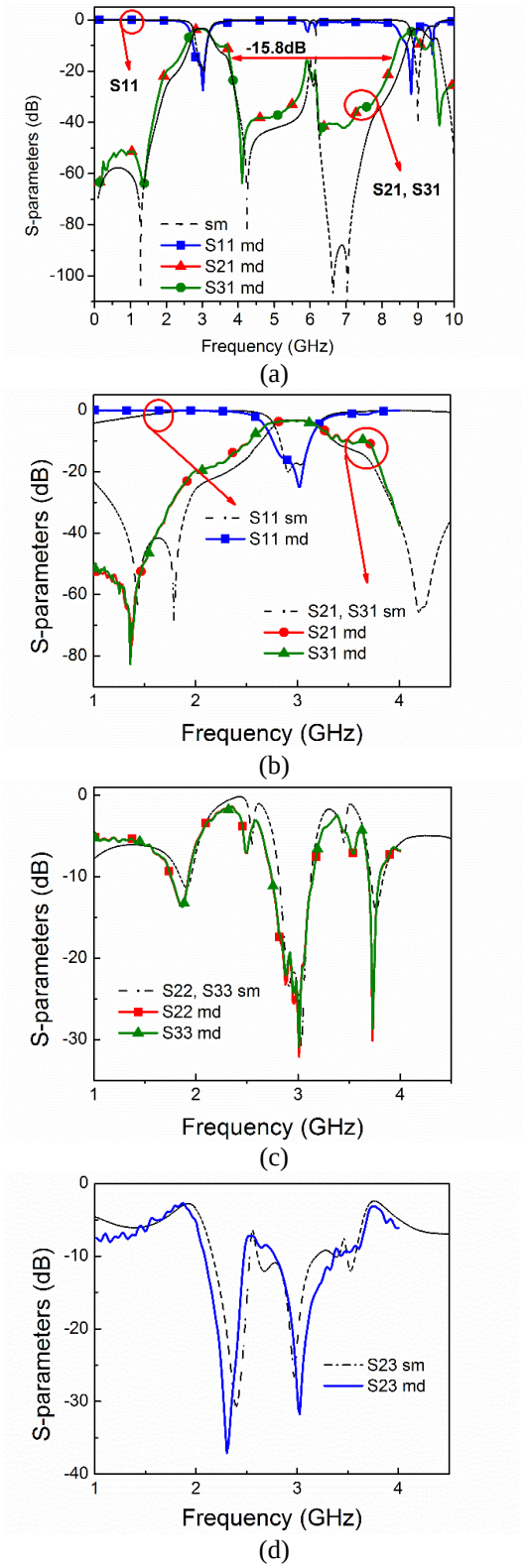


Fig. 4. Measured vs. Simulation response of CPLFD (sm = simulated, md = measured). (a) Wide-band response, (b) transmission characteristics in narrow band, (c) output port return loss, and (d) output port isolation.

Figure 5 depicts the measured amplitude imbalance/ difference (|S21| - |S31|) and phase imbalance/difference ($\angle$S21 - $\angle$S31) at the output ports of the CPLFD over the achieved operational FBW. At 3 GHz, the amplitude difference is 0.036 dB and phase difference is -0.59° which implies that the divided signals at the two output ports have almost same amplitude and phase. Simultaneous good even and odd mode responses can be noted in the circuit designed through proposed methodology.

Table 2 presents a comparison of the presented work with some previous works. It may be noted from Table 2 that [2, 3, 7] offer sharp skirt (having transmission zeros) at the cost of bigger order of the filter and higher IL. The IL in [8] is low with no transmission zeros and reactive elements have been employed. Similarly in [9], even and odd mode responses are not simultaneously good. The work presented here achieves good input port match and low IL while maintaining reasonable output port match and return loss with two transmission zeros.

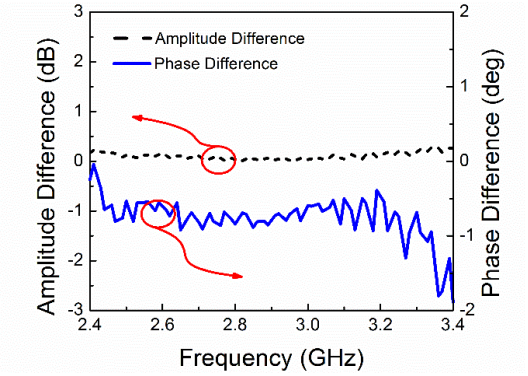


Fig. 5. Amplitude and phase imbalance at output port.

Table 2. Comparison of proposed work with previous work

Works	Parameters								
	Order	BPF Type	Isolation Elements	Input Port RL (dB)	IL (dB)	Output Port RL (dB)	Isolation (dB)	FBW (%)	Transmission Zeros
[2]	4	Quasi-elliptical filter	R	~25	6.4	~25	15	4	4
[3]	3	Quasi-elliptical filter	R	20	3.99	20	20	6.5	2
[7]	5	Coupled line filter	3dB Hybrid	30	5.2	30	25	9.8	2
[8]	-	Single coupled line section	LCR	30	3.15	30	23	Not given	None
[9]	2	Coupled line filter	R	27	5.5	27	24	14.9	None
	4	Coupled line filter	R	25	6.8	25	24	15.2	2
This work CPLFD	2	Coupled line filter	TL, R	25	3.45	29	31	15.3	2

V. CONCLUSION

A new design methodology has been proposed for filtering divider with a transmission line and resistor as isolation elements which ensures simultaneous good even and odd mode response. As a first step, coupled line filter (CPLF) was designed and matched to 70.7Ω in the simulation and was subsequently integrated in the PD with a 50Ω extended TL and a 100Ω resistor as isolation elements. The designed coupled line filtering divider (CPLFD) was fabricated and measured response was good over a FBW of 15.3% at the design frequency of 3 GHz. A sufficiently wide out-of-band response was achieved for most practical purposes with two transmission zeros in the vicinity of the pass-band. The achieved S-parameters (S11/S22/S33, S21/S31, S23) in the designed prototype were in reasonably good agreement with simulation results, authenticating the proposed technique.

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