FPGA Based Fast Bartlett DoA Estimator for ULA Antenna Using Parallel Computing

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Abstract **─** This paper presents a design and implementation of a structure which uses Bartlett Direction of Arrival (DoA) algorithm and a receiver system on Altera Cyclone IV and Cyclone III FPGAs. First of all, a software defined radio (SDR) that has 4 simultaneous inputs, is designed. All data used in this study are obtained by using this radio system. Then one of the FPGA is configured as antenna simulator and the other one is used for implementing Bartlett DoA estimation algorithm. Bartlett DoA estimation algorithm is developed completely in parallel and compared with a previous study which is performed sequentially on an FPGA using NIOS processor. The designs are tested by using 4-element Uniform Linear Array (ULA) antenna. Implemented hardware is compared in terms of DoA calculation speed and the sources that occupy on the FPGA. Furthermore, the paper has significant improvement in calculation duration thereby achieving lower response latency compared with previously published similar works.

Index Terms **─** Bartlett algorithm, direction of arrival estimation, FPGA, parallel computing.

I. INTRODUCTION

An antenna array is a system consisted of singular antenna elements that are designed to behave like a single antenna used to receive and/or radiate the electromagnetic waves. These antenna arrays are also known as smart antennas have the ability to estimate Direction of Arrival (DoA) as well as high directivity, high gain, formable radiation pattern features. In addition, having the features to prevent co-channel fading and to create low side lobe level (SLL) abilities, interference is reduced by antenna arrays. With the help of these features, the use of antenna arrays on systems such as surveillance radar, ground penetrating radar, sonar, ultrasonic imaging, seismic data processing and medical imaging offers significant advantages [1-5].

Detection of the direction of an incident signal received by an antenna array is called DoA estimation. This bases on process actualized with processing the relative phase difference between incident signals onto antenna elements. DoA estimation is widely used in such applications like mobile communication, radar, and sonar etc. [6]. There are three principles of DoA estimation methods named conventional spectral-based, subspace spectral-based, and statistical methods. The most popular conventional spectral-based methods are Bartlett, Capon, First Order Forward Prediction, Maximum Entropy [7], Deterministic and Stochastic Maximum Likelihood (DML, SML) [8]. The popular subspace spectral-based methods are Multiple Signal Classifying (MUSIC), Min-Norm and Weighted Subspace Fitting (WSF). And the statistical methods are Estimation of Signal Parameters via Rotational Invariance Techniques (ESPRIT), Root-MUSIC and Root-WSF [8-11]. These methods have really long calculation processes. Since operations are performed one after the other in the sequential calculation, the DoA estimation calculations like eigenvalue decomposition in subspace-based methods and covariance calculation operation which is the most common operation in all of the methods, cost huge calculation duration [12]. Because of having the ability of parallel calculation, an FPGA could be employed to solve these DoA Estimation problems much faster than a classical microprocessor.

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Table 1: Comparison of the studies in literature in terms of calculation duration and utilized logic elements

Ref.	Structure / Method	Number of Antenna	Calculation Duration (μs)	Utilized Logic Elements
[13]	Sequential / New EVD Structure-based MUSIC DoA Estimation	4 ULA	27.64	14609
[14]	Sequential / ROM Based Unitary MUSIC processor with spatial smoothing	4 ULA	30.59	12007
[14]	Sequential / ROM Based Unitary MUSIC processor without spatial smoothing	4 ULA	57.11	12995
[14]	Sequential / ROM Based Unitary MUSIC processor without spatial smoothing	8 ULA	373.99	29472
[15]	Sequential / ARM-Cortex Core microprocessor based MUSIC DoA Estimator	8 ULA	2560	-
[16]	Parallel-Sequential / Butterfly FFT Core based on DSP48E microprocessor	8 ULA	-	33961
[17]	Sequential / A coordinate rotation digital computer (CORDIC) based Sum&Delay DoA Estimator	16 ULA	768	-
[18]	Sequential / MicroBlaze soft processor based Bartlett DoA Estimator	8 UCA	684	2349
[18]	Parallel-Sequential / Bartlett DoA Estimator	8 UCA	312.13	165
[18]	Parallel-Sequential / FFT DoA Estimator	8 UCA	104.8×10^3	7434

In literature, due to the aim of the application (like improve calculation speed, reduce complexity or optimal hardware consumption), the results could be various. The most attractive studies about DoA estimation based on an FPGA with Uniform Linear Array (ULA) and Uniform Circular Array (UCA) are presented in Table 1.

In this study, working with data taken from the real environment is aimed. For this purpose, a data collection hardware is designed. The collected dataset is stored on a PC. Then with the next hardware implementation, a DoA estimation is done by using the dataset which was collected from antenna array in a real environment. The proposed system is a highly parallel calculating method. For each angle, the values in the pseudo spectrum are calculated fully parallel but the calculation of whole pseudo spectrum needs 181 sequences.

In the second section, the design of the systems is presented. In the third section, the proposed DoA estimation method, Bartlett, is introduced. In the fourth section, the architecture in the FPGA is presented, in the next section, the performance comparison is done. In the last section, the conclusions are presented.

II. SYSTEM DESIGN

Usage of the FPGAs in a system does not guarantee that this system is going to be faster. The most important point of an FPGA usage is the ability of parallel computing. So, for a significant improvement in process duration, it is an obligation to use of parallel calculation ability of the FPGAs. Furthermore, to make an existing algorithm possible to run parallel, it has to be investigated and optimized deeply.

The established system to estimate DoA calculation has two stages. The first stage is for data collecting from the real environment. That hardware collects data from 4 quarter wave antenna and saved into a PC. These recordings are done in an open area to avoid reflections. In this stage, the FPGA evaluation board is employed as 4 channel shift register and serial communicator.

In the second stage, Bartlett DoA estimation is done by using the recorded data. In this stage, two FPGA evaluation board are used. The first FPGA evaluation board is employed to simulate an antenna array output by using the data collected in the first stage. The dataset comprises the environmental noise, the mutual coupling effects of the antennas in the array. So, it is possible to examine the DoA estimation algorithms in the laboratory environment as if they are done in the real world. The setups used in these stages are presented in Fig. 1.

In the first stage, an RF Front-End and data collector structure has been designed. The signals received from 4 monopole antenna elements are amplified by a preamplifier (PA). This amplifier has 4 channels that have equal and fixed gain about 10 dB. The amplified received signal is applied to a mixer IC. Each channel has own mixer ICs, but all of the local oscillator (LO) inputs of mixers are fed from same crystal oscillator with the same length of a path. The obtained intermediate frequency (IF) signal at the output of mixer IC is filtered by a crystal resonator filter (CRF). The IF signal with the frequency of 2MHz, has been amplified by IF amplificator (IF). ADA daughter board (ADA-GPIO) by Altera Company is used as the analog-digital converter. The IF signals received from 4 channels are converted into 8-bit digital data in 40 MSPS speed using two ADA-GPIOs. The ADA-GPIOs are connected to Altera DE0 Board. For the rest of the operations, Altera DE0 Board is used.

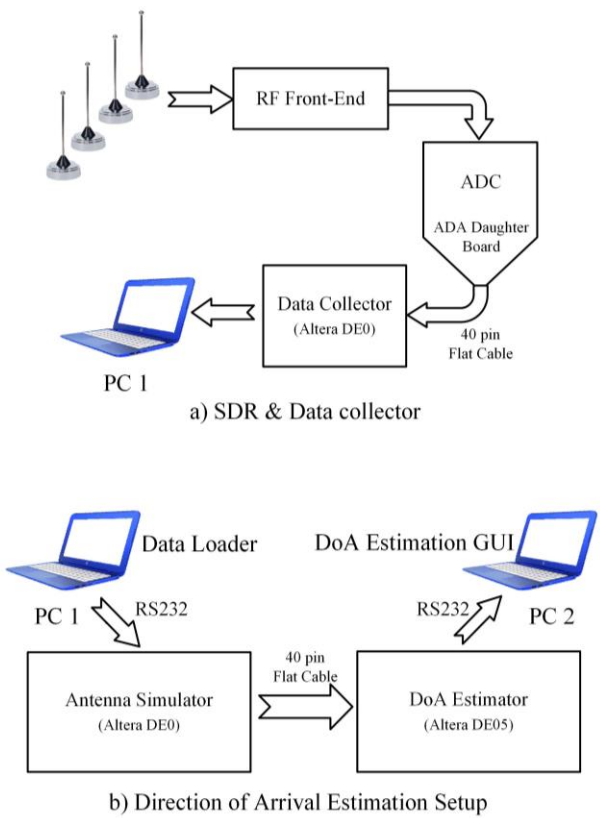

Fig. 1. (a) The first stage: Data acquisition setup. (b) The second stage: DoA estimation setup.

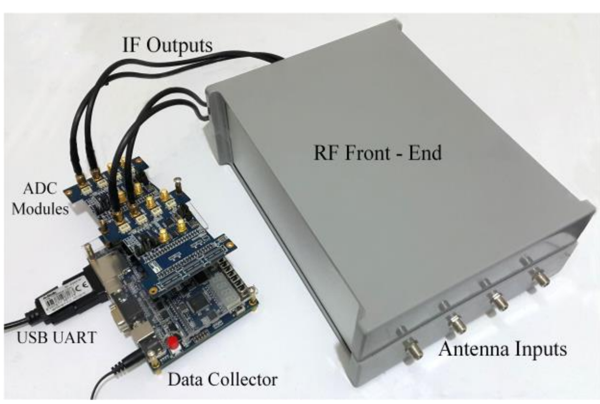

Fig. 2. Software defined radio & data collecting.

The measurements are done in an open area to avoid reflections. They are performed while two unmodulated narrowband transmitters are at different angles and results are recorded. The measurement set-up whose flow chart is presented in Fig. 1 (a) is shown in Fig. 2. The block diagram of data collection hardware whose picture is seen in Fig. 2 is presented in Fig. 3.

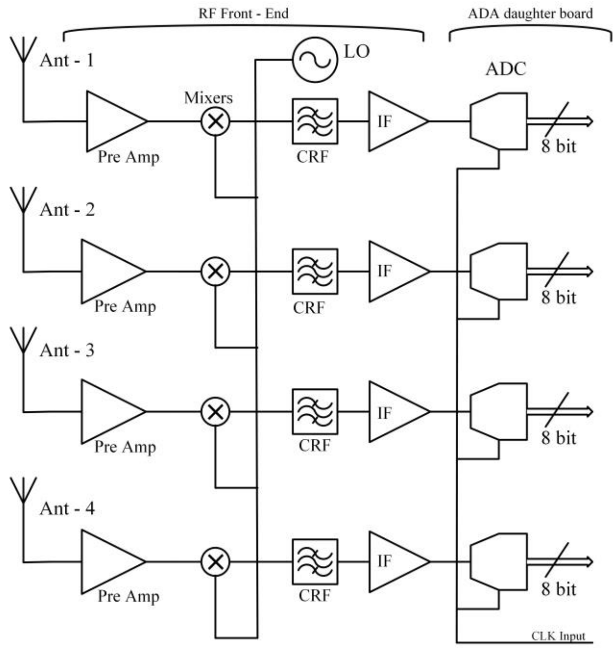

Fig. 3. The block diagram of RF Front-End & data collecting setup.

After the ADA-GPIOs the IF signal is digitized and taken into the FPGA. Each of these digitized samples has taken into shift registers from each channel simultaneously. Totally 480 samples are transferred to a PC via Universal Synchronous/Asynchronous Receiver/ Transmitter (USART) when 120 samples are collected from all of the inputs. To avoid mistakes, a header consists of 5 bytes to the beginning of the stream and a checksum byte at the end of the stream is added. So, each transfer sequence consists of 486 bytes. The block diagram of the shift register used for data collection operations and implemented by VHDL codes for FPGA DE0 board is presented in Fig. 4.

When the user asks from the software in the PC to take a capture, the software looks for a header, then collects 480 bytes of data after the header, and after receiving the checksum, compares it with the calculated one. If the checksum byte comparison is confirmed the collected data is stored on the hard disk with date, time and an explanatory text. Else, whole instructions mentioned above are repeated.

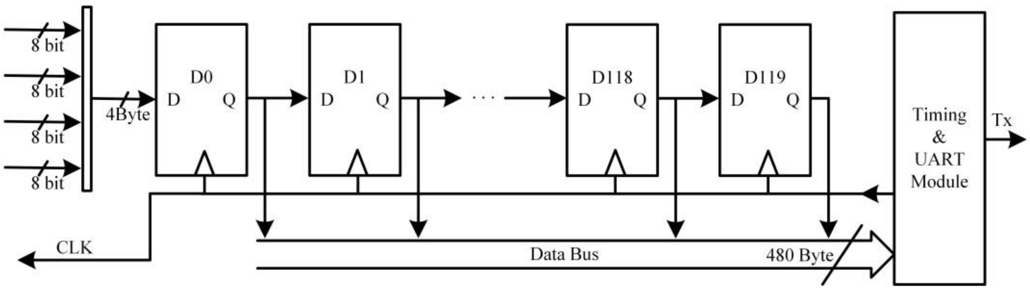

Fig. 4. The block diagram of data collector implemented on the FPGA.

Since there is a filtration operation during the IF signal amplification, the IF signal almost consists of a single frequency at 2MHz. So, the digital IF signal recorded on the hard disk is subject to the mathematical models given in Equation (1):

$$U[n] = A\cos\left(2\pi f_0 \frac{n}{f_s} + \varphi\right), \tag{1}$$

where A represents signal amplitude, n represents the sample index changing between 1 and 120, f_0 represents the operating frequency (2MHz), f_s represents the sampling frequency (40MHz).

All measurements are done in open area due to avoid unwanted reflections. A signal generator connected to a monopole antenna is used as the signal source. In measurements, two unmodulated signal sources are settled up to various angles and 120 samples of 4 IF signals are recorded. Totally 480 records are taken for each setup and stored on a PC to use in DoA estimation stage.

In the second stage, the recorded data in the first stage is embedded into DE0 board which simulates an antenna array or an RF front-end outputs. The data is sequentially driven to the outputs through Circular Shift Register (CSR). The antenna simulator whose flowchart is presented in Fig. 1 (b) is demonstrated as a block diagram in Fig. 5.

DoA estimation is done on DE2-115 development and education board of Altera Company. The DoA estimation is achieved by using Bartlett algorithm on DE2-115 board. Results are transferred to a PC via a UART protocol. They are observed and saved by a GUI software on a PC. The inner connection between DE0 and DE2-115 is done by using 40 pin Integrated Drive Electronics (IDE) cable. But to avoid interferences into the data signals in IDE cable, it is screened with a grounded aluminum foil. The measurement set-up is presented in Fig. 6.

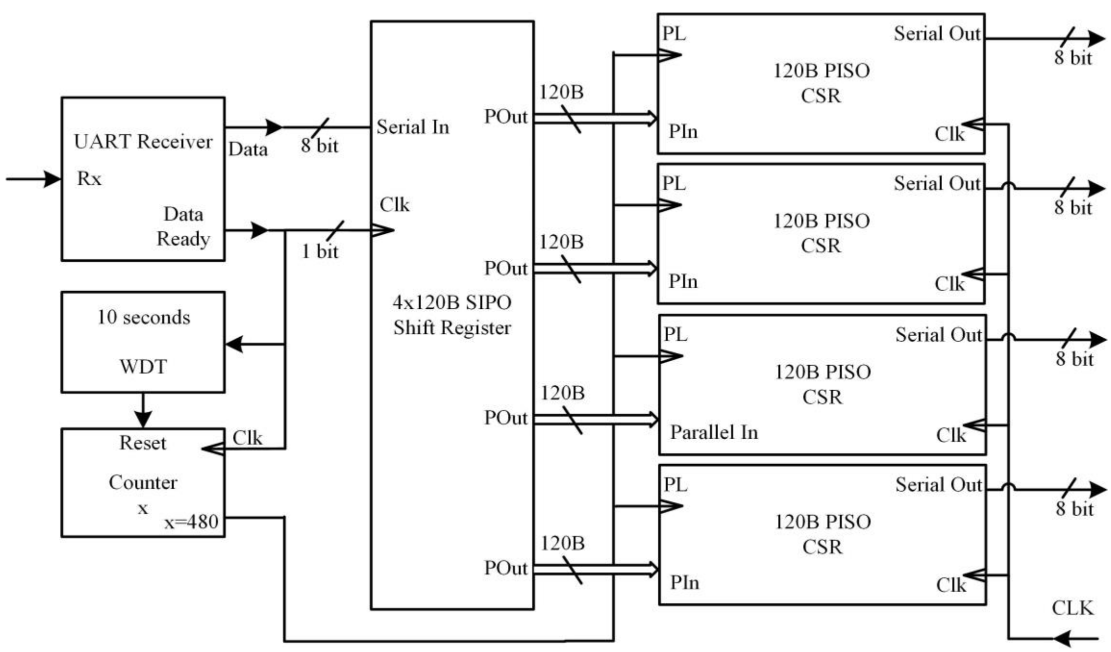

Fig. 5. The block diagram of the antenna simulator implemented on the FPGA.

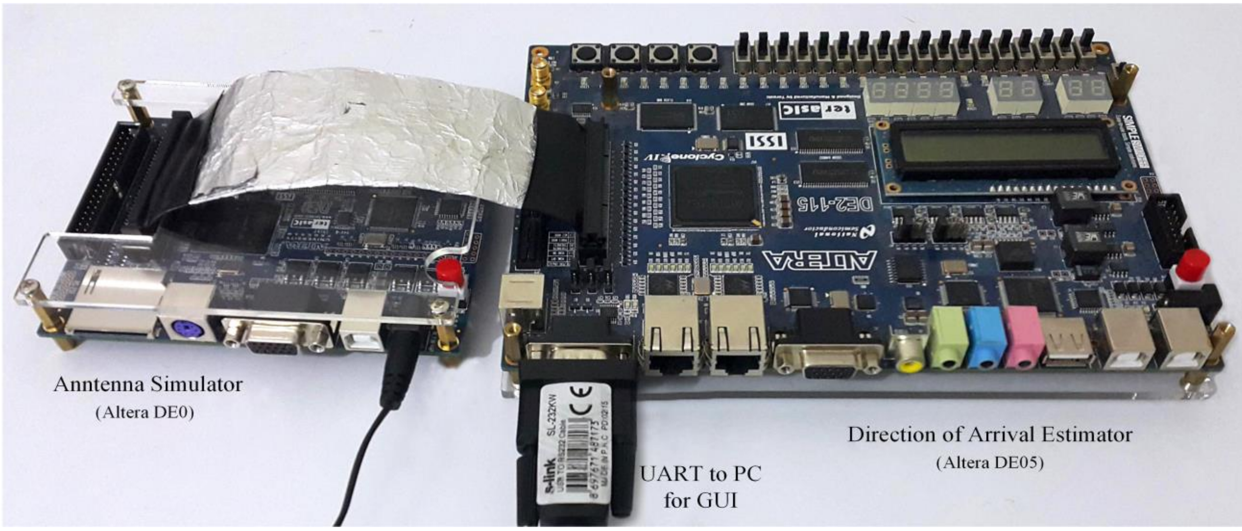

Fig. 6. DoA estimation set-up.

III. BARTLETT DoA ESTIMATION

In the Bartlett spectral estimation method, the power maintained from the antenna array is calculated as the function of θ, and a spatial spectrum is obtained. Local maximums are determined in this spatial spectrum. The result is the power coming through $P_B(\theta)$. This value is obtained by Equation (2) [9]:

$$P_B(\theta)=\frac{S_\theta^H \times R \times S_\theta}{N^2}, \tag{2}$$

where S_θ represents steering vector for θ, N represents the number of antenna elements forming ULA antenna and R represents covariance matrix of the array. $(\ )^H$ represents Hermitian conjugate of a vector. S_θ and Hermitian conjugate of S_θ are given by Equation (3) [9]:

$$\begin{aligned} S_\theta[n]&=e^{jnkd\sin(\theta)} \\ S_\theta^H[n]&=e^{-jnkd\sin(\theta)} \end{aligned} \qquad n=0\to N-1. \tag{3}$$

In Equation (3) the k represents the wave number which is equal to $2\pi/\lambda$. And the d represents distances between antenna elements in the ULA. This value is chosen as $\lambda/2$. The N parameter which represents the number of antenna elements in ULA antenna is 4 in this study.

To make Equation (2) suitable for parallel computing, following simplifications are done:

$$\begin{aligned} P_B(\theta)&=\frac{1}{N^2}\sum_{n=1}^{4}\sum_{m=1}^{4}S_\theta[n].R[n,m].S_\theta^H[m], \\ P_B(\theta)&=\frac{1}{N^2}\sum_{n=1}^{N}\sum_{m=1}^{N}e^{jn\pi\sin(\theta)}.e^{-jm\pi\sin(\theta)}.R[n,m], \\ P_B(\theta)&=\frac{1}{N^2}\sum_{n=1}^{N}\sum_{m=1}^{N}e^{j(n-m)\pi\sin(\theta)}.R[n,m]. \end{aligned} \tag{4}$$

In Equation (4), it is possible to observe that the minimum and maximum value of n-m is 1-N and N-1 respectively. So if a W vector is defined as in Equation (5), the Bartlett DoA estimation formula in Equation (4) can be presented as in Equation (6):

$$W_\theta[p]=e^{jp\pi\sin(\theta)} \qquad p=1-N\to N-1. \tag{5}$$

$$P_B(\theta)=\frac{1}{N^2}\sum_{n=1}^{N}\sum_{m=1}^{N}W[n-m].R[n,m]. \tag{6}$$

The new vector W_θ is calculated in this study by the Equation (7):

$$\begin{aligned} W_\theta&=\begin{bmatrix} e^{-j3\pi\sin(\theta)}, e^{-j2\pi\sin(\theta)}, e^{-j\pi\sin(\theta)}, \\ 1,\ e^{j\pi\sin(\theta)}, e^{j2\pi\sin(\theta)}, e^{j3\pi\sin(\theta)} \end{bmatrix}, \\ W_{\theta r}&=\begin{bmatrix} \cos(-3\pi\sin(\theta)),\cos(-2\pi\sin(\theta)),\cdots \\ \cdots,\cos(2\pi\sin(\theta)),\cos(3\pi\sin(\theta)) \end{bmatrix}, \\ W_{\theta i}&=\begin{bmatrix} \sin(-3\pi\sin(\theta)),\sin(-2\pi\sin(\theta)),\cdots \\ \cdots,\sin(2\pi\sin(\theta)),\sin(3\pi\sin(\theta)) \end{bmatrix}. \end{aligned} \tag{7}$$

This process conducted on Bartlett DoA estimation algorithm resembles the calculation of the power radiated from the antenna array towards each angle physically. However, the obtained value from a certain direction not only contains the signal sources in the direction, but also the signal sources from side lobes slightly [19].

IV. HARDWARE IMPLEMENTATION

The signals obtained in the physical environment have real values. However, DoA estimation algorithms need also imaginary parts of the signals as input [20]. Since the IF is a narrow band signal, the polar expression of IF signal can be expressed as in Equation (8):

$$\begin{aligned} U[n]&=Ae^{j\left(\frac{2\pi f_0}{f_s}n+\varphi\right)}, \\ U[n]&=A\left(\cos\left(\frac{2\pi f_0}{f_s}n+\varphi\right)+j\sin\left(\frac{2\pi f_0}{f_s}n+\varphi\right)\right). \end{aligned} \tag{8}$$

The collected data is the real part of the value in Equation (8). In order to derive imaginary part needed in Bartlett algorithm, several methods could be employed. For example, the imaginary part is equal to $(A^2 - R^2)^{1/2}$ where A is the envelope of signal and R is the real values. But both "envelope determination" and "square root operation" cause extra calculation duration.

In this study, some trigonometric manipulations are done to obtain the imaginary part of the signal by using just basic four operations. The well-known sum and subtraction formulas of cosine presented in Equation (9) form the basis of the manipulations:

$$\begin{aligned} \cos x + \cos y &= 2\cos\left(\frac{(x+y)}{2}\right).\cos\left(\frac{(x-y)}{2}\right), \\ \cos x - \cos y &= -2\sin\left(\frac{(x+y)}{2}\right).\sin\left(\frac{(x-y)}{2}\right). \end{aligned} \tag{9}$$

Since the f_s and f_0 are chosen as 40MHz and 2MHz respectively, two sequential samples ((n-1)th and nth) can be expressed as in Equation (10):

$$\begin{aligned} U[n] &= A\cos\left(\frac{2\pi f_0}{f_s}n+\varphi\right) = A\cos\left(\frac{\pi}{10}n+\varphi\right), \\ U[n-1] &= A\cos\left(\frac{2\pi f_0}{f_s}(n-1)+\varphi\right) = A\cos\left(\frac{\pi}{10}(n-1)+\varphi\right). \end{aligned} \tag{10}$$

In order to obtain an expression contains sinus function, it is clear that subtraction formulas should be used:

$$\begin{aligned} DeltaU &= U[n-1] - U[n], \\ DeltaU &= A\left(\cos\left(\frac{\pi}{10}(n-1)+\varphi\right) - \cos\left(\frac{\pi}{10}n+\varphi\right)\right), \\ DeltaU &= -A\times 2\times \sin\left(\frac{\pi}{10}\left(n-\tfrac{1}{2}\right)+\varphi\right)\times\sin\left(-\frac{\pi}{20}\right), \end{aligned} \tag{11}$$

Hence sinus expression can be written as in Equation (12) [21]:

$$\begin{aligned} A\ \sin\left(\frac{2\pi f_0}{f_s}\left(n-\tfrac{1}{2}\right)+\varphi\right) &= \frac{DeltaU}{2\times\sin\left(\frac{\pi}{20}\right)} = \frac{\left(U[n-1]-U[n]\right)}{0.3129}, \\ A\ \sin\left(\frac{2\pi f_0}{f_s}\left(n-\tfrac{1}{2}\right)+\varphi\right) &\simeq \frac{25}{8}\times\left(U[n-1]-U[n]\right). \end{aligned} \tag{12}$$

It can be seen that the sample index of the obtained imaginary part (sinus expression) is (n-0.5). To make real part concurrently with the imaginary part, some manipulations need on real part. In order to obtain a cosine expression with (n-0.5) sample index, the sum of two sequential samples in Equation (10) can be calculated:

$$\begin{aligned} SumU &= U[n-1] + U[n], \\ SumU &= A\left(\cos\left(\frac{\pi}{10}(n-1)+\varphi\right) + \cos\left(\frac{\pi}{10}n+\varphi\right)\right), \\ SumU &= A\times 2\times\cos\left(\frac{\pi}{10}\left(n-\tfrac{1}{2}\right)+\varphi\right)\times\cos\left(-\frac{\pi}{20}\right), \end{aligned} \tag{13}$$

The cosine expression can be written as in Equation (14):

$$\begin{aligned} A\ \cos\left(\frac{2\pi f_0}{f_s}\left(n-\tfrac{1}{2}\right)+\varphi\right) &= \frac{U[n-1]+U[n]}{2\times\cos\left(-\frac{\pi}{20}\right)} = \frac{U[n-1]+U[n]}{1.9754}, \\ A\ \cos\left(\frac{2\pi f_0}{f_s}\left(n-\tfrac{1}{2}\right)+\varphi\right) &\simeq \frac{1}{2}\times\left(U[n-1]+U[n]\right). \end{aligned} \tag{14}$$

As a result of manipulations seen above, the real and imaginary values can be expressed as in Equation (15) [21]:

$$\begin{aligned} U_r[n-0.5] &= \frac{1}{2}\left(U[n-1]+U[n]\right), \\ U_i[n-0.5] &= \frac{25}{8}\left(U[n-1]-U[n]\right). \end{aligned} \tag{15}$$

First, the *U[n]* data is taken from ADC into the FPGA. Then the real and imaginary parts of this data are calculated by the help of the Equation (15). And two shift registers are added to record U_r and U_i on each clock cycle. The calculation method of imaginary and real parts of the data on the FPGA is presented as a block diagram in Fig. 7.

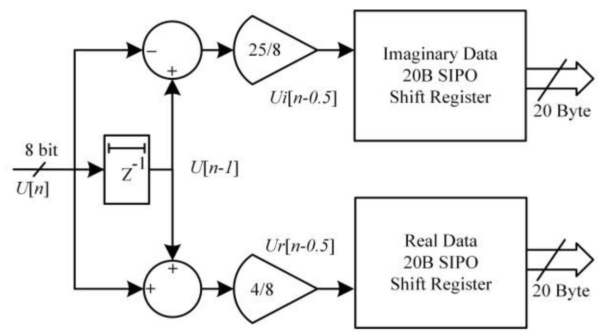

Fig. 7. The extraction of imaginary - real values and shift registers on the FPGA.

Next step is the calculation of the covariance matrix. The input matrix of covariance calculation consists of 20 samples obtained from each antenna outputs. Since there are 4 sensors in the ULA antenna, the dimension of input matrix is 4×20.

The covariance of X_a and X_b vectors are calculated as in Equation (16) [22]:

$$Cov(X_a, X_b) = E\left[\left(X_a - E(X_a)\right)^H \times \left(X_b - E(X_b)\right)\right]. \tag{16}$$

Here, E operator shows the average of the related vector. $(\ )^H$ symbol indicates the Hermitian conjugate of the concerned vector. The E operator executes the operations in Equation (17):

$$E(U) = \frac{1}{N}\sum_{n=1}^{N} U[n] = \frac{1}{N}\sum_{n=1}^{N}\cos\left(\frac{2\pi f_0}{f_s}n+\varphi\right). \tag{17}$$

A practical identity about the sum of cosine series is presented in Equation (18) [23]:

$$\sum_{n=1}^{N}\cos(xn+\varphi) = \frac{\cos\left(\frac{N+1}{2}x+\varphi\right)\sin\left(\frac{N}{2}x\right)}{\sin\left(\frac{x}{2}\right)}. \tag{18}$$

If the transformation in Equation (18) is performed in the Equation (17), the Equation (19) is obtained:

$$E(U)=\frac{1}{N}\sum_{n=1}^{N}\cos\left(\frac{2\pi f_0}{f_s}n+\varphi\right)$$
$$E(U)=\frac{\cos\left((N+1)\frac{\pi f_0}{f_s}+\varphi\right)\sin\left(\frac{N\pi f_0}{f_s}\right)}{N\sin\left(\frac{\pi f_0}{f_s}\right)}. \quad (19)$$

In order to make the mean value of U presented in Equation (19) zero, $\sin(N\pi f_0/f_s)$ has to be equal to zero. Therefore $N\pi f_0/f_s$ needs to be equal to πk which makes sinus zero:

$$\text{if} \quad \frac{N\pi f_0}{f_s}=\pi k \quad \text{then } E(U)=0 \quad \text{for } k=0,1,2...$$
$$N=\frac{f_s}{f_0}k=\frac{40}{2}k=20k. \quad (20)$$

The sampling frequency is chosen as a multiple of the signal frequency. Additionally, the number of samples taken into shift registers is chosen as 20 which is a multiple of the ratio between the sampling frequency and the signal frequency. These predilections make the average of the related vector zero as presented in Equation (20).

That circumstance eliminates the average calculations in the covariance calculation. So, the Equation (16) could be reconstructed as in Equation (21):

$$Cov(X_a,X_b)=E\left[(X_a)^H\times(X_b)\right]. \quad (21)$$

This provides a reduction in the FPGA source consumption and calculation duration. As the number of sensors in the ULA antenna is 4, the covariance matrix has to be 4×4 size as shown in Equation (22):

$$R=\begin{bmatrix} R[1,1] & R[1,2] & R[1,3] & R[1,4] \\ R[2,1] & R[2,2] & R[2,3] & R[2,4] \\ R[3,1] & R[3,2] & R[3,3] & R[3,4] \\ R[4,1] & R[4,2] & R[4,3] & R[4,4] \end{bmatrix}. \quad (22)$$

The covariance matrix is diagonally symmetric [22]. In order to get calculations simple, $R[2,1]$, $R[3,1]$, $R[4,1]$, $R[3,2]$, $R[4,2]$ and $R[4,3]$ are not calculated, only the conjugant value of related element is assigned. The real and imaginary parts of R matrix are calculated as shown in Equation (23) [21]:

$$R[a,b]=R_r[a,b]+j\times R_i[a,b],$$
$$R_r[a,b]=\frac{1}{20}\sum_{n=1}^{20}\begin{pmatrix} U_r[a,n]\times U_r[b,n] \\ +U_i[a,n]\times U_i[b,n] \end{pmatrix}, \quad (23)$$
$$R_i[a,b]=\frac{1}{20}\sum_{n=1}^{20}\begin{pmatrix} U_r[a,n]\times U_i[b,n] \\ -U_i[a,n]\times U_r[b,n] \end{pmatrix},$$

where $U[a,n]$ is n^{th} sample taken from the a^{th} antenna:

$$P_B(\theta)=\frac{1}{N^2}\sum_{n=1}^{N}\sum_{m=1}^{N}W[n-m].R[n,m],$$
$$P_{B\,real}(\theta)=\frac{1}{16}\sum_{n=1}^{4}\sum_{m=1}^{4}\left(W_r[n-m].R_r[n,m]-W_i[n-m].R_i[n,m]\right), \quad (24)$$
$$P_{B\,imag}(\theta)=\frac{1}{16}\sum_{n=1}^{4}\sum_{m=1}^{4}\left(W_r[n-m].R_i[n,m]+W_i[n-m].R_r[n,m]\right),$$

with the covariance matrix R, DoA strength estimation for any angle θ is calculated by using Equation (6).

In order to reduce calculation process, the W vector is obtained from a pre-calculated table. Integer is used as the class in all process. The whole block diagram of the Bartlett DoA system is shown in Fig. 8 [21].

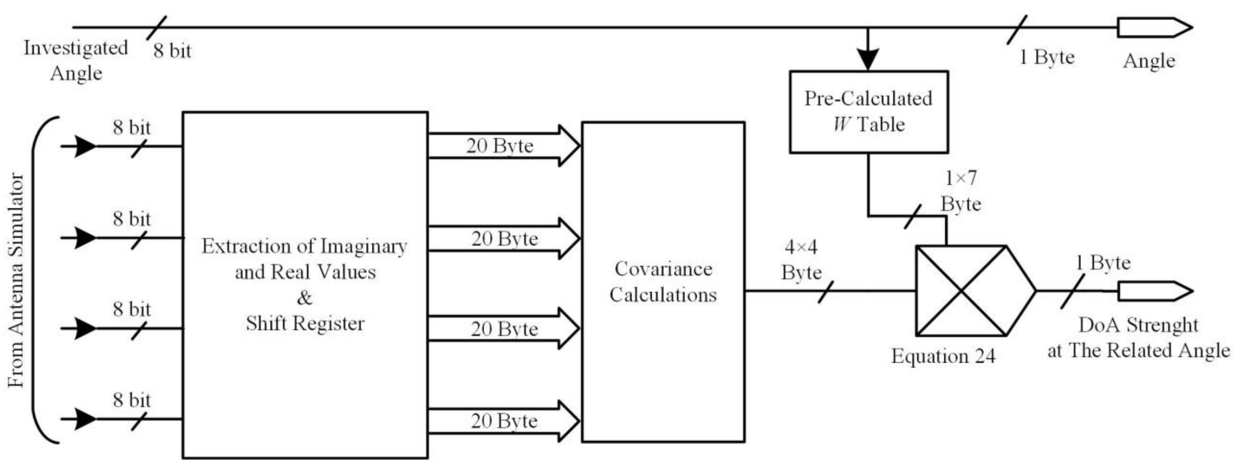

Fig. 8. Block diagram of the Bartlett DoA algorithm on the FPGA.

The data obtained from this system is kept by a sphift register and transferred to a PC via serial port. The DoA estimation results are observed by a GUI on a PC. Figure 9 shows a screenshot of GUI taken from a PC [21].

The most important disadvantage of this method is the data transfer process. The process of transferring data from the FPGA to a PC is slower compared to the DoA estimation calculations. Designing a system that creates control outputs according to the DoA results on the same device, (means a fully embedded system) would provide significant benefits in real-time applications.

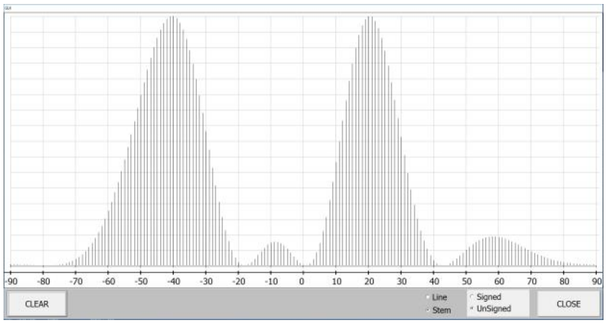

Fig. 9. Screenshot of the GUI shows DoA estimation results on pseudo-spectrum.

V. PERFORMANCE COMPARISON

In this algorithm, DoA estimation is done for 181° pseudo-spectrum between -90° and 90°. By means of 1° increase in each clock pulse, the incoming signal existence from the related angle is calculated. Thereby, for the DoA estimation of the whole pseudo-spectrum, 181 clock pulse is needed. Since the working frequency is 225MHz, the DoA estimation duration for the whole pseudo-spectrum calculations is about 804.44 ns.

In the study [18], the Bartlett DoA Estimation algorithm had done using MicroBlaze soft processor on an FPGA as presented in Table 2 Structure No. 1. When the scripts in the study [17] are considered, it is seen that the DoA estimation of the whole pseudo-spectrum is calculated with 118193 clock pulse.

Besides, the custom VHDL in the study [18] is designed in two types, as Parallel-Sequential Bartlett DoA Estimator and Parallel-Sequential FFT DoA Estimator; presented in Table 2 with Structure No. 2 and 3 respectively. The DoA estimation durations on FPGA are presented as 312.13 µs and 104825 µs respectively. Clock cycle, calculation duration, utilized logic elements for the study [17] and the proposed method are given in Table 2.

VI. CONCLUSION

This paper presents design and implementation of a fast parallel Bartlett DoA estimation hardware on an FPGA. Since the signals in the study are collected from the real world, the data involves all the effects such as noise, reflections, and interferences between antennas. Moreover, its comparison with Bartlett DoA estimation algorithm, which is created by using MicroBlaze soft processor and custom design VHDL codes, was done.

Table 2: Comparison of the proposed method and the study [17] in calculation duration

Structure No.	**Structure / Method / Reference**	**Clock Cycle**	**Calculation duration (µs)**	**Utilized Logic Elements**
1	Seq. MicroBlaze soft processor based Bartlett DoA estimator [18]	118193	684	2349
2	Parallel-Seq. Bartlett DoA estimator [18]	53929 (Estimate)	312.1	165
3	Parallel-Seq. FFT DoA estimator [18]	18.19×10^6 (Estimate)	104.8×10^3	7434
4	Parallel Presented in this paper	181	0.804	8467

Besides the improvements in the FPGA technology, the optimization process on the algorithm has an important role on the duration reduction of calculation. It can be seen that DoA estimation which is performed by using parallel calculation, provides a considerable increase in calculation speed. This provides a significant improvement over the similar studies found in literature. By making modifications to covariance matrix calculation and steering vector usage, it has become possible to scan the whole pseudo-spectrum in just 181 clock pulses. The DoA estimation hardware developed in this study is presented as Structure 4 in Table 2. By comparing based on calculation duration, the Structure 4 produces results in 0.034% of calculation duration of Structure 1 (2920 times faster than Structure 1), 0.49% of calculation duration of Structure 2 (205 times faster than Structure 2) and 0.01% of calculation duration of Structure 3 (9241 times faster than Structure 3). Although calculation durations could give an impression, this information has a close relation between working frequency, it has also a relation between improvements in the technology. In order to obtain more objective results, the clock cycle count need to be compared. If a comparison is done based on clock counts, it could be seen clearly that Structure 4 is 653 times faster than Structure 1. This radical decrease in the calculation is occurred because of the algorithm optimizations and adaptation of sequential algorithm into parallel. In this study, arrangements on Bartlett algorithm and imaginary part obtaining method is performed. These are the major effects on achieving the low latency. The results are promising for future works about a standalone fast DoA estimator system on an FPGA.

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