Wideband Multi-Port Network Integrated by 3-dB Branch-Line Couplers

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Abstract **─** The design of a multi-port network integrated by symmetrical alignment of four 3-dB branch-line couplers (BLCs) for wideband communication applications is presented. The BLC is designed with the implementation of stub impedance at each port's transmission line and defect ground structure (DGS) underneath the shunt branches of BLC to improve bandwidth. The designs of the BLC and the multi-port network are performed by using CST Microwave Studio, a three-dimensional (3D) electromagnetic wave simulator. The designed wideband BLC and multi-port are fabricated, and their wideband performances of 2.3 to 5.3 GHz are verified.

Index Terms **─** Branch line coupler, defect ground structure, multi-port, stub impedance, wideband.

I. INTRODUCTION

The rapid development of wireless communication demands high-performance devices for future 5th Generation (5G) technologies considering spectrum below 6 GHz and higher than 6 GHz, which yet to be finalized. This future 5G-communication system is envisioned as the possibility of boundless and continuous communication and connection among any devices and machines at anywhere and anytime [1]. This vision prompts an enormous challenge to design and plan a network and front-end system that include antenna and RF/microwave components.

The multi-port network is one of the RF/microwave components that have been growing steadily, owing to its outstanding potential for the future technology of 5G. The multi-port network can be used in various wireless communication applications, such as a modulator or demodulator for modulation and demodulation purposes [2-4]. The common modulator is basically built up based on the mixer-based approach, which involves active devices that require biasing voltage, resulting in design complexity [2-3]. Therefore, in favor of reducing the complexity of the design, the multi-port network integrated by passive devices such as the quadrature coupler and power divider is proposed as an alternative to the common modulator.

An impressive bandwidth of a multi-port network has been demonstrated by [5], which implements the design technique of the multilayer microstrip-slot. It consists of two substrates, which are sandwiched by three layers of conductive copper. The microstrip patches on the top and bottom layer are broadside-coupled through slotlines that are placed at the middle layer. In contrast to its wide bandwidth, the design faces the production of an air gap and misalignment between the two substrates. Furthermore, it may encounter a connection problem to other components since the ports are located at both top and bottom layers.

Consequently, to deal with these drawbacks in [5], the branch line coupler (BLC) is an alternative that can be used in the multi-port network configuration. However, the conventional BLC is only capable of offering limited bandwidth. Accordingly, various studies have been conducted, specifically to improve the bandwidth performance of BLC. As reported in [6], a technique of implementing the defect ground structure (DGS) onto the single-section BLC is used. The purpose of implementing the DGS is to increase the phase velocity delay [6, 7, 8] of the design that contributes to bandwidth improvement. Another technique in improving the bandwidth is by implementing the stub impedance onto the single-section BLC as proposed in [9]. The implementation of stub allows the design to have wideband operation with very flat coupling [9].

However, the bandwidth of the proposed single-section BLC reported in [6, 9] is still inadequate. Therefore, to overcome the limited bandwidth in [6, 9], another technique can be used to broaden the bandwidth, which is by increasing the sections of BLC [10]. Thus by considering the design techniques in [6, 9, 10], it is worth applying the stub impedance and DGS to the two-section BLC, whereby well-tuning the stub impedance, matching can be improved and, consequently, bandwidth is enhanced. In addition, the DGS also contributes to improving the bandwidth.

In this article, a multi-port network integrated by four two-section 3-dB BLCs is proposed. The BLC is designed with the implementation of DGS underneath the shunt branches at the ground plane and stub impedance at each port's transmission line, which can operate across 2.3 to

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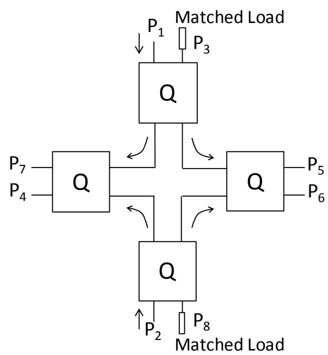
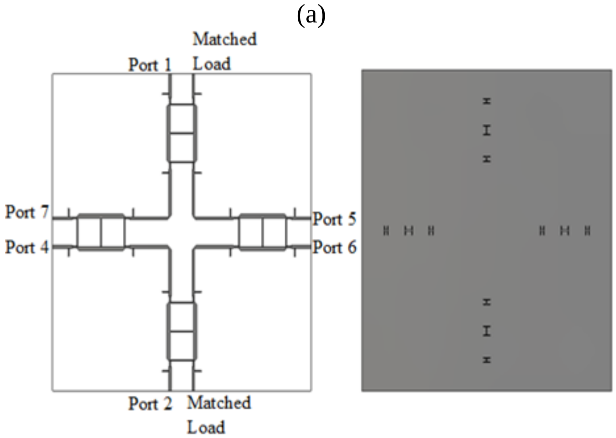
5.3 GHz. The designs of the two-section 3-dB BLC and multi-port network are executed in an electromagnetic simulator known as CST Microwave Studio. The performance of the scattering parameters and phase characteristics of the proposed multi-port network and BLC are studied and verified experimentally.

II. DESIGN OF MULTI-PORT NETWORK

The proposed multi-port network is formed by integrating four BLCs that are denoted as blocks of 'Q', which are placed symmetrically as in Fig. 1 (a). Its CST generated layout is shown in Figs. 1 (b) and (c) and is integrated by the enhanced BLCs. As shown in Fig. 1, the input ports are depicted by Ports 1 and 2, while other corresponding ports are labelled as Ports 4 to 7. The other two remaining unused ports (Ports 3 and 8) are terminated by 50Ω to maintain well-matching operation of the multi-port network.



(a)



(b)

Fig. 1. (a) The configuration of the proposed multi-port network, and the CST generated layout of proposed multi-port network; (b) top and (c) bottom view.

The proposed design is initially utilizing two-section BLC with step impedance at four ports as presented in the following Fig. 2. The implemented step impedance is functioning as one of the matching techniques in this proposed design to reduce the reflections occurred at the transition between ports' transmission lines and BLC's branches. Referring to [10], the initial characteristic impedances of a and d are set to 157Ω, while, b and c are set to 29Ω. These initial values are determined through the deliberation on the correlation of cascade parameters, transmission and reflection coefficients, perfect matching isolation at design frequency with $S_{11} = S_{41} = 0$, the equal power ratio between output ports (Port 2 and 3) and the assumption of the characteristic impedance, Z_0 = 50Ω. Afterward, the optimization is performed to improve bandwidth in which the finalized impedances are a = c = d = 121Ω and b = 35Ω.

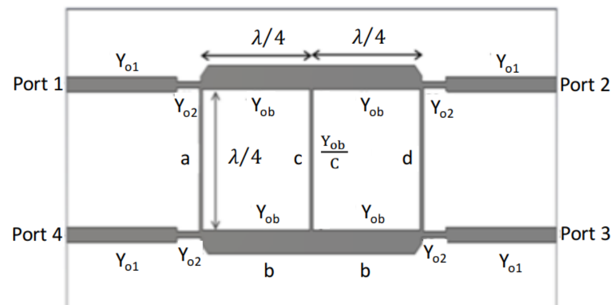


Fig. 2. The CST generated layout of the two-section branch-line coupler with step0 impedance at ports.

The step impedance at four ports is denoted by width, W_1 and length, L_1, which has admittance of Y_{02}. This Y_{02} can be determined from the following relation of (1) [11]:

$$\left[\left(1+\frac{Y_{01}}{Y_{02}}\right)\cos^2\Delta-\left(1+\frac{Y_{01}}{Y_{02}}\right)\sin^2\Delta\right]Y_{01}^2+\left[\frac{1}{\cos\Delta}\right]\frac{1+C}{1-C}Y_{01}-\left[\left(1+\frac{Y_{01}}{Y_{02}}\right)\cos^2\Delta-\left(1+\frac{Y_{01}}{Y_{02}}\right)\sin^2\Delta\right]=0, \quad (1)$$

where Y_{01}, Δ and C are the admittance of the port transmission line, load impedance and numerical coupling coefficient, accordingly. In this design, Y_{01} is fixed at $1/Z_0$ = 0.02 S. Meanwhile, to obtain equal power division at Ports 2 and 3, C is set to 0.707. Thus, admittance of Y_{02} is 0.0083 S, which corresponds to 120Ω. Whereas, the Δ is set to 0 to have maximally flat solution with a perfect matching at center frequency, which also enhanced the bandwidth performance. Whilst, the initial dimension of step impedance length, L_1 is λ/4. However, transmission loss has occurred, which degrades the performance of the coupler. Hence, the length is varied and optimized, where the optimal length of $\lambda/73$ is accomplished.

Afterward, stub impedance is placed at 0.07λ from the branch that determined through the conducted parameter sweep to avoid junction discontinuities and improve matching, which corresponds to 3.7mm as shown in Fig. 3. Theoretically, the half-wavelength stub impedance with higher impedance is required in order to achieve optimal performance [11]. However, the half-wavelength of stub impedance in this design has contributed to mismatch problems. Thus, the length of stub impedance, L_{s1} is varied and optimized that resulting the optimal length of 50λ/657. While, its optimized impedance is 121Ω. Next, the H-shaped DGS is employed at the ground plane of the BLC, where the DGS employment can improve the bandwidth performance due to its slow-wave characteristic [16]. The implementation of DGS is only suitable on the microstrip line with higher impedance. Therefore, it is placed underneath each of parallel branches that having impedance of 121Ω as shown in Fig. 3. The DGS characteristic impedance, Z_D, is expressed as in (2) [6]:

$$Z_D = Z_0 Z_{in}, \tag{2}$$

where Z_{in} is the input impedance towards DGS section that can be determined by the following Equation (3):

$$Z_{in} = Z_0\sqrt{\frac{1+|\Gamma|}{1+|\Gamma|}}, \tag{3}$$

where Γ is the reflection coefficient prior to the addition of DGS in the design. Hence, Z_D for this design is 122Ω. Whilst, the initial length of the DGS, L_m is computed by referring to [13]. In order to improve the performance of S_{21}, the size of DGS at the center is designed to be slightly larger, which also influences the flatness of the phase difference performance.

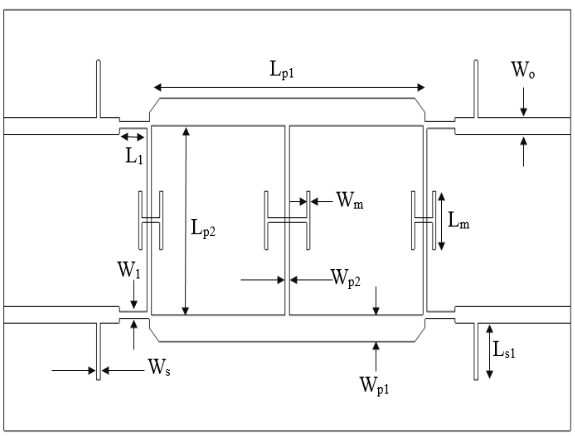


Fig. 3. The CST generated layout of the proposed design with its dimensions.

As shown in Fig. 3, the width dimensions of W_o, W_1, W_{p1} and W_{p2} that correspond to the respective impedances of 50Ω, 120Ω, 35Ω and 121Ω are determined by the microstrip line equation as expressed in the following (4) [12]:

$$\frac{W}{h} = \frac{2}{\Pi}\left[\frac{377\Pi}{2Z_0\sqrt{\varepsilon_r}} - 1 - \ln\left(\frac{377\Pi}{Z_0\sqrt{\varepsilon_r}} - 1\right) + \frac{\varepsilon_r - 1}{2\varepsilon_r}\left\{\ln\left(\frac{377\Pi}{2Z_0\sqrt{\varepsilon_r}} - 1\right) + 0.39 - \frac{0.61}{\varepsilon_r}\right\}\right], \tag{4}$$

where h and ε_r are the thickness of the substrate and dielectric constant, respectively. Meanwhile, the length dimensions of L_{p1}, L_{p2}, L_1 and L_{S1} are calculated to correspond to λ/2, λ/4, λ/73 and 50λ/657, accordingly. The wavelength, λ is computed from (5) [12]:

$$\lambda = \frac{c}{f\sqrt{\varepsilon_e}}, \tag{5}$$

where c, and f are the respective speed of light and design frequency. Meanwhile, ε_e is the effective dielectric constant that can be presented by (6) [12]:

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\frac{1}{\sqrt{1 + 12h/W}}. \tag{6}$$

The width dimension of DGS, W_m is determined from Z_D = 122Ω using the following Equation (7) [14-15]:

$$Z_D = 60 + 3.69\sin\left[\frac{(\varepsilon_r - 2,22)\Pi}{2.36}\right] + 133.5\ln(10\varepsilon_r)\sqrt{\frac{W_m}{\lambda_0}} + 2.81\left[t - 0.11\varepsilon_r(4.48 + \ln\varepsilon_r)\right]\left(\frac{W_m}{h}\right)\ln\left(\frac{100h}{\lambda_0}\right) + 131.1(1.028 - \ln\varepsilon_r)\sqrt{\frac{h}{\lambda_0}} + 12.48(1 + 0.181\ln\varepsilon_r)\frac{W_m/h}{\sqrt{\varepsilon_r - 2.06 + 0.85(W_m/h)^2}}. \tag{7}$$

The proposed design of 3-dB BLC is realized utilizing a substrate of Rogers RO4003C. This substrate has 0.508 mm thickness with 0.017 mm copper cladding at both sides, a 3.38 dielectric constant and a very low loss tangent of 0.0027. The coupler, as shown in Fig. 3, has final optimized dimensions of W_o = 1.15 mm, W_1 = 0.48 mm, W_{p1} = 1.85 mm, W_{p2} = 0.4 mm, W_m = 0.3 mm, W_s = 0.35 mm, L_1 = 2.2 mm, L_{p1} = 26.28 mm, L_{p2} = 13.14 mm, L_{s1} = 4.0 mm. The BLC design occupies an area of 54 mm x 29 mm.

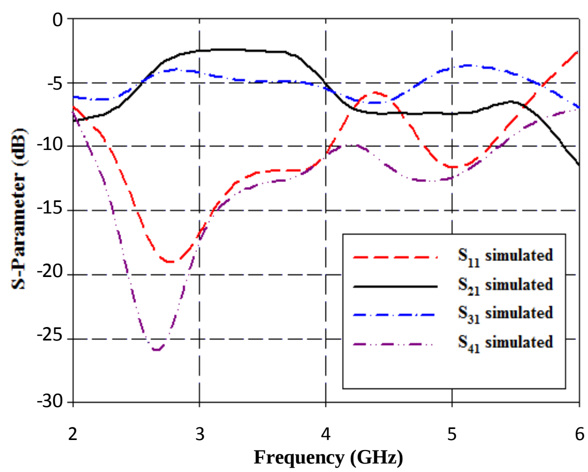
III. RESULTS AND DISCUSSION

The performance of the BLC and multi-port are evaluated based on the S-parameters and phase characteristics, which are split into two subsections. The initial design of the two-section BLC with step impedance at ports is assessed and presented, followed by the enhanced BLC design with DGS and stub impedance, and the multi-port network design. The proposed BLC and multi-port network designs are fabricated and verified through the measurement using a vector network analyzer (VNA) in the laboratory.

A. Analysis and verification of enhanced two-section branch-line coupler

The first concern involves the performance of the initial design of the two-section BLC with step impedance at ports, whose configuration is presented in Fig. 2. Figure 4 (a) shows the initial BLC's simulated performance of the S-parameter. It can be observed that the good return loss and isolation performance of greater than 10 dB are both within 2.5 to 4 GHz. Furthermore, the transmission coefficient of S_{21} demonstrates the performance of -3 dB with oscillated deviation of -2 dB across the similar frequency range. Meanwhile, this initial design offers an oscillation of S_{31} between -4 dB and -5 dB.

The plotted response in Fig. 4 (b) shows the simulated performance of phase differences among output ports. It demonstrates that the simulated phase difference between Port 2 and 3 is at 90° ± 10° between 2.5 and 4 GHz. The performance of this initial design of the proposed coupler is summarized in Table 1. This initial design offers a fractional bandwidth of 46% compared to a conventional single-section BLC and conventional two-section BLC presented in [10] with respective bandwidths of 32% and 34.4%.



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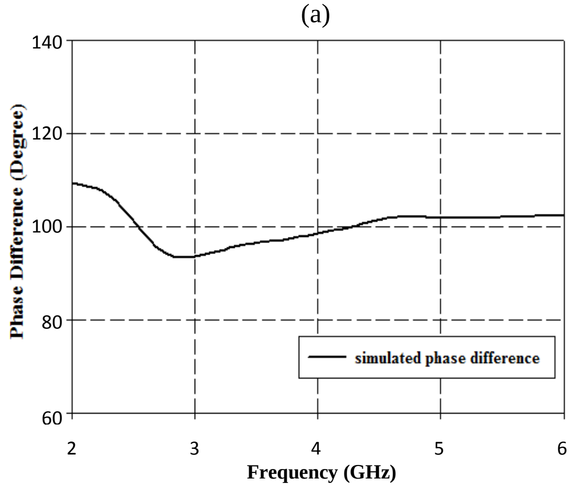


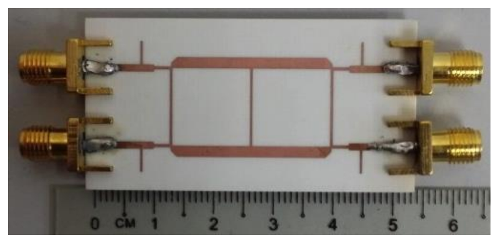
(b)

Fig. 4. The simulated (a) S-performance and (b) phase difference of the initial design of two-section BLC with step impedance at ports.

Following this, the proposed design of a two-section BLC with stub impedance and DGS is fabricated. Figure 5 shows the fabricated prototype of the proposed two-section BLC, where each port is connected to subminiature A (SMA) connectors. Its wideband performance is then practically measured in the laboratory using a vector network analyzer (VNA). Afterward, the comparison is made in terms of the simulated and measured S-parameters and phase characteristic performances.

Table 1: The simulated performance of the initial design of two-section BLC with step impedance at ports

Parameters	Performance
S_{11} & S_{41}	≤ -10 dB
S_{21}	-3 dB ~ -5 dB
S_{31}	-4 dB ~ -5 dB
Phase Difference	90° ± 10°
Operating Frequency	2.5 GHz – 4 GHz



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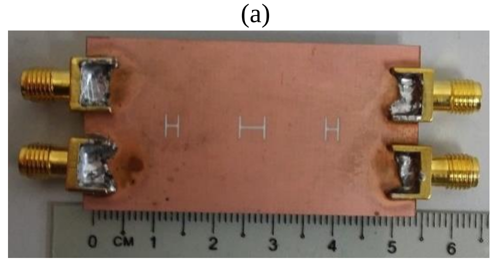
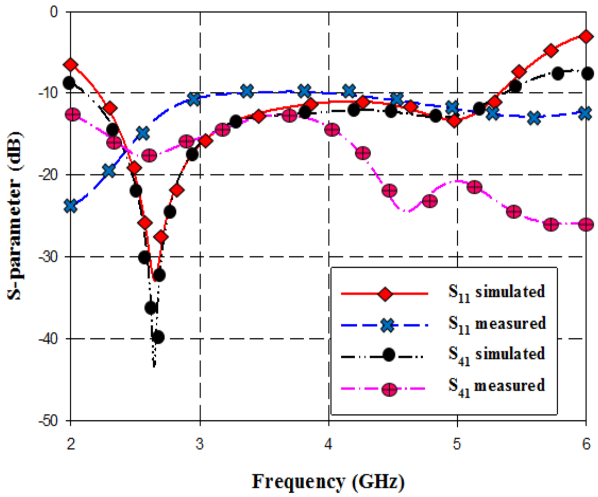


(b)

Fig. 5. The prototype of the two-section BLC design with DGS and stub impedance: (a) front and (b) bottom view.

Figure 6 and Fig. 7 depict the simulated and measured performances of the proposed BLC, which exhibits a good wideband operation of 2 GHz bandwidth, between 2.3 and 5.3 GHz. Within this frequency range, the simulated and measured reflection coefficient performances of S_{11} at Port 1 are lower than -10 dB. Meanwhile, the isolation performance is better than 11 dB.

The simulated and measured coupling coefficients show the respective performance between 2.2 dB to 5 dB and 4 dB to 5 dB, as plotted in Fig. 6 (b). Moreover, the simulated and measured transmission coefficients between the through port (Port 2) and the input port (Port 1), which are presented by S_{21}, are fluctuating within -2.4 dB to -5 dB and -3.2 dB to -4.5 dB, accordingly. Meanwhile, the plotted responses in Fig. 7 show that the simulated and measured phase difference between output ports are 90° ± 2° and 90° ± 4°, accordingly. These S-parameter and phase difference performances are then summarized in Table 2 for better comparison purposes. The analysis of the reflection coefficient, transmission coefficient, coupling coefficient, isolation and phase characteristic performance of the proposed coupler summarized in Table 2 shows that employing stub impedance improves the matching of the designed coupler.



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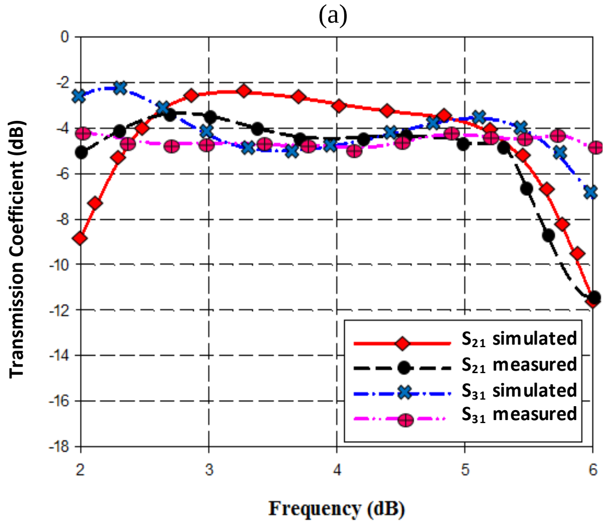


(b)

Fig. 6. The simulated and measured (a) S_{11} and S_{41}, and (b) transmission coefficients of S_{21} and S_{31} of the proposed BLC with stub impedance and DGS.

Consequently, stub impedance also improves the performance of phase characteristic with less deviation compared to the initial design. Meanwhile, the implementation of DGS enhances the bandwidth performance of the proposed coupler with a fractional bandwidth of 79% compared to the initial design, which exhibited a bandwidth of 46%. Following the wideband performance verification of the proposed BLC, the next concern is to evaluate the performance of the multi-port network.

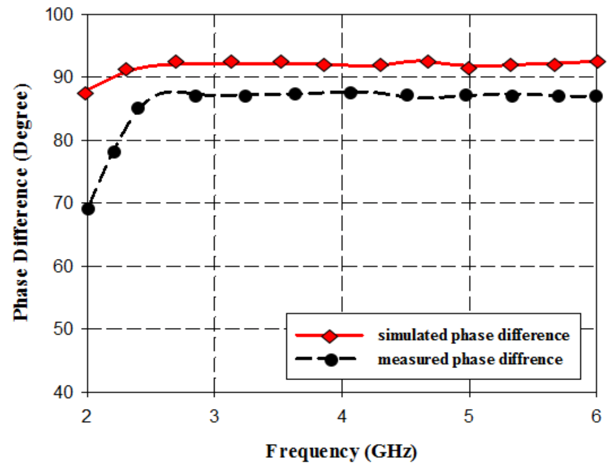


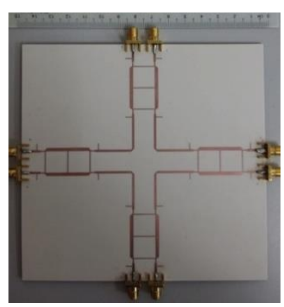
Fig. 7. The simulated and measured phase difference of the proposed BLC with stub impedance and DGS

Table 2: The performance of the designed BLC with stub impedance and DGS

Parameters	Performance	
	Simulation	Measurement
S_{11}	$\leq$ -10 dB	
S_{21}	-2.4 dB ~ -5 dB	-3.2 dB ~ -4.5 dB
S_{31}	-2.2 dB ~ -5 dB	-4 dB ~ -5 dB
S_{41}	$\leq$ -11 dB	
Phase Difference	90° ± 2°	90° ± 4°
Operating Frequency	2.3 GHz – 5.3 GHz	

B. The performance of multi-port network

The proposed multi-port network is fabricated using Rogers RO4003C substrate, where each port is connected to subminiature A (SMA) connectors for testing purposes, as shown in Fig. 8. The multi-port design has a total size of 144 mm x 144 mm.



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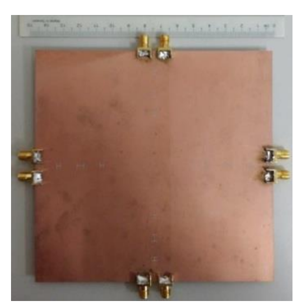


(b)

Fig. 8. The photography of the fabricated multi-port network: (a) top view and (b) bottom view.

As observed in Fig. 9 to Fig. 11, the proposed multi-port network has a good wideband performance of 2.3 to 5.3 GHz. The performances of simulated and measured reflection coefficients of S_{11} and S_{22} are less than -10 dB, as denoted by the plotted responses in Fig. 9. These indicate good return loss performance at the input ports of Port 1 and Port 2. The next concern involves the simulated and measured transmission coefficients referenced against Port 1 and Port 2, which are presented in Fig. 10.

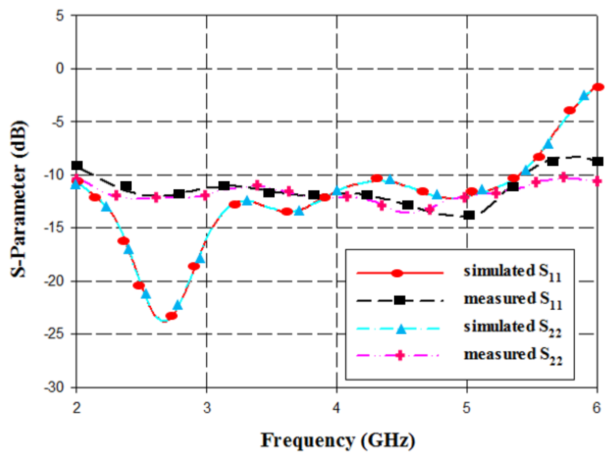


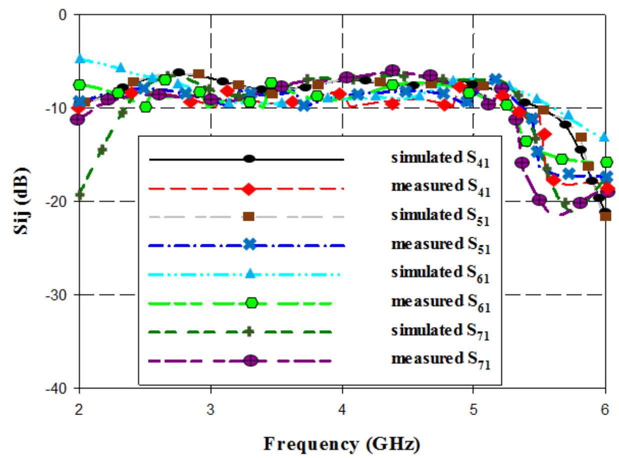
Fig. 9. Simulated and measured reflection coefficients of the proposed multi-port network.

Referring to Fig. 10 (a), the simulated and measured transmission coefficients referenced to Port 1 oscillate in the range of -8 dB ± 1.5 dB, and -8 dB ± 2 dB across 2.3 to 5.3 GHz, respectively. Meanwhile, Fig. 10 (b) presents the respective simulated and measured transmission coefficients referenced to Port 2, which fluctuate around -8 dB ± 1.8 dB and -8 dB ± 2 dB in a similar frequency range. As expected, the measured results exhibit more deviation compared to the simulation. This can be attributed by the inaccurate width of transmission lines that may occur during the fabrication process. The slight changes in the width of transmission lines can affect the performance of the overall design. However, the measurement results still demonstrate good performance across the designated frequency range.

Then, the analysis proceeds with performances of the phase characteristics. The phase characteristics can be analyzed based on Equation (8):

$$\angle S_{\Delta ijk}(\deg ree) = \angle S_{ij}(\deg ree) - \angle S_{4k}(\deg ree), \quad (8)$$

where i = 4, 5, 6, 7, j = 1, 2, and k = 1, 2. Figure 11 (a) shows that the performances of the simulated and measured phase characteristics of $S_{\Delta 711}$ and $S_{\Delta 421}$ are 90° ± 10° from 2.3 to 5.3 GHz, respectively. Meanwhile, the simulated and measured phase characteristics of $S_{\Delta 511}$, $S_{\Delta 621}$ and $S_{\Delta 721}$ are approximately 0° within the similar range frequency. Next, the simulated and measured phases of transmission coefficients $S_{\Delta 611}$ and $S_{\Delta 521}$ are -90° ± 10°.



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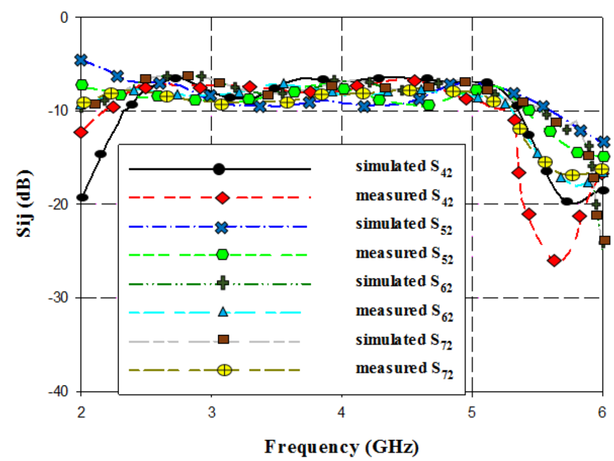
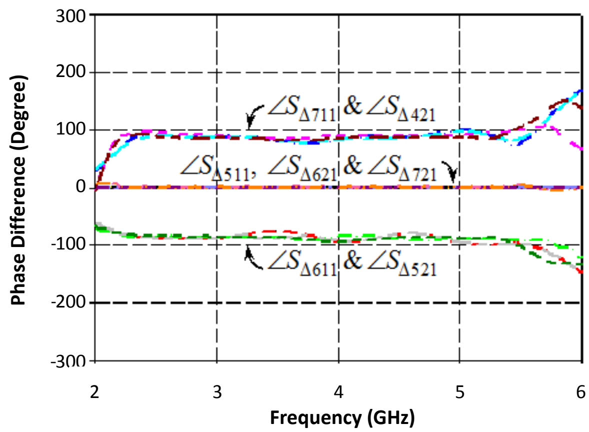


(b)

Fig. 10. Simulated and measured transmission coefficients, S_{ij} (i = 4, 5, 6, 7 and j = 1, 2): (a) S_{i1} and (b) S_{i2} of the proposed multi-port network.

Figure 11 (b) depicts the simulated and measured phases of transmission coefficients that are plotted against the transmission coefficient phase of S_{42}. As seen in the plotted graph, the simulated and measured transmission coefficient phases of $S_{\Delta 412}$, $S_{\Delta 512}$, $S_{\Delta 622}$ and $S_{\Delta 722}$ are -90° ± -10° across 2.3 to 5.3 GHz. The simulated and measured transmission coefficients' phases of $S_{\Delta 612}$ and $S_{\Delta 522}$ show the worst deviation of 20° from 180° within the similar frequency range. Meanwhile, the phase of transmission coefficient of $S_{\Delta 71}$ is almost 0°. Based on Figs. 9 to 11, the multi-port network demonstrates comparable performance between simulation and measurement, which offers a good wideband operation with a fractional bandwidth of 79%, covering 2.3 to 5.3 GHz.



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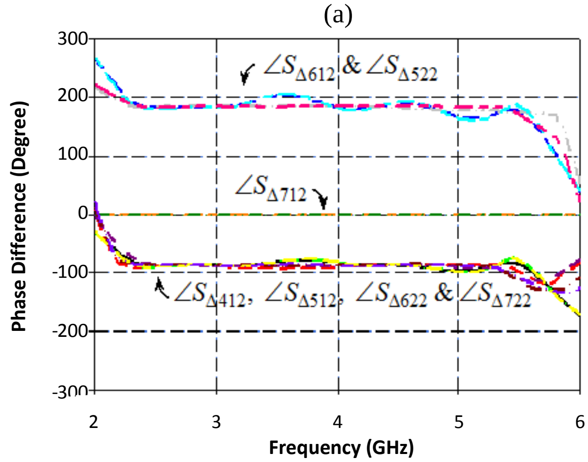

(b)

Fig. 11. Multi-port network's simulated and measured phase characteristics referenced to: (a) $\angle S_{41}$ and (b) $\angle S_{42}$.

IV. CONCLUSION

A wideband multi-port network integrated by four two-section BLCs implemented with DGS and stub impedance techniques with an overall size of 144 mm x 144 mm has been presented. The design and optimization have been executed using CST Microwave Studio, an electromagnetic (EM) simulator. The performances of transmission coefficients, reflection coefficients and phase characteristics of the designed couplers and multi-port network have been assessed and analyzed. The designed two-section BLC and multi-port network have been fabricated. Their wideband performances from 2.3 to 5.3 GHz are proven via measurement in the laboratory. This wideband multi-port can be employed in the front-end system of various wireless communication applications as a modulator or demodulator for modulation and demodulation purposes.

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