Design of a Compact Hybrid Branch Line Coupler with 2-D Implementation of Stepped Impedance Transmission Lines of High Impedance Ratio for Wide Range of Harmonic Suppression

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Abstract ─ In this paper stepped impedance transmission line (TL) structure is adopted by using proposed unorthodox technique to design a hybrid branch line coupler (HBLC) in micro-strip technology. In addition to achieving good fractional bandwidth of 30% and size reduction of 56%, the proposed technique ensures a high impedance ratio (M) over a wide range of electrical lengths of the high-Z low-Z (stepped impedance) sections. Maintaining high M ensures a good harmonic suppression of the proposed design up to $9f_0$ (f_0 is the design frequency which is 1GHz for this work). Experimental verification of the proposed technique is demonstrated by designing an HBLC at 1GHz. Experimental and simulation results show excellent conformance.

Index Terms ─ Harmonic suppression, high impedance low impedance structure, hybrid branch line coupler, impedance ratio.

I. INTRODUCTION

Branch line coupler, owing to its capability to couple a fraction of signal with controllable power and phase makes it essential for many useful applications at microwave and milli-metric frequency regimes. A quadrature hybrid branch line coupler (HBLC) is one such device which equally splits the signal with a 90° mutual phase difference and may be particularly useful in applications like antenna array network, balanced mixers and amplifiers, phase shifter, crossover design [1] and Butler matrix design [2] etc. In addition, it may also be used in signal sensing and monitoring in measurement equipment (like network analyzers) and radio frequency front-ends (RFFE) of most radar and communication systems. A passive directional branch line coupler (BLC) is usually employed for the task to couple a fraction of the signal and monitor its frequency and phase without disturbing the main transmission. Conventional BLCs, however suffer from bigger size (due to quarter-wave (λg/4) transmission lines (TL)) and inherent narrow bandwidth typically around 8-10% [3-4] making it not suitable for ever reducing, bandwidth hungry modern systems. Yet another disadvantage is its poor ability to suppress the higher order harmonics which are produced due to periodic nature of λg/4 transformers. These unwanted harmonics may adversely affect the performance of other sub-systems/systems. Thus, good out-of-band response is highly desirable. Different design strategies have been proposed to address the above mentioned shortcomings in the conventional HBLC [5-26]. A careful analysis of the literature reveals that simultaneous achievement of miniaturization, wide operational bandwidth and reasonable out-of-band rejection has not been possible and there has always been a tradeoff between these characteristics. For example a fairly wide bandwidth (BW) of 49% and 50.9% was achieved in [5-6] respectively at the cost of size enlargement to almost three fold with no harmonic suppression. On the contrary, a BLC with size reduction of 67.5% was reported in [7] operational over a very narrow BW of 1.8%, again with no harmonic suppression. A lot of efforts have been done in order to strike a balance between the two extremities of BW and size as mentioned above, without considering harmonic suppression [8-17] and with harmonics suppression as design parameter [18-26]. In [8-9], a fractional bandwidth (FBW) of 10% was achieved with size reduction of 33% and 55% by employing defected ground structure (DGS) and cascaded transmission line (TL) with open stub techniques respectively. Comb-line structure was used in place of λg/4 transformers in [10], and asymmetrical T-shaped TLs in [11] to improve the FBW to 23% and 24% with area reduction rate of 22.6% and 55% respectively. Yet another BLC design technique utilizing the polar curves [12] was used to achieve a FBW of 30% with an overall size of 50% of the conventional BLC. Recently, remarkable size reduction of about 62% has been achieved by employing high-low

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impedance TL in substrate integrated suspended line technology [13] and cascaded slow-wave cells in [14]. The reported FBWs for the two design approaches were 20% and 32% respectively. Artificial TLs based design approaches were presented in [15-17]. A BLC with area reduction of 47% operational over a FBW of around 40% was achieved in [15] by utilizing a combination of dual TL and π-model technique, while in [16] only dual TL and in [17] only π-model based artificial TL were implemented to achieve a size reduction of 63.9% and 62% and FBW of 43% and 33% respectively. In all the above cited works [5-17], out-of-band performance or harmonic suppression capability of the BLC was not considered which has become another important design consideration in modern systems.

Many researchers have proposed different design techniques to achieve good out-of-band performance of the BLC at the cost of FBW and/or circuit size [18-26]. Reference [18] used slow-wave methodology by using four high-low impedance resonant cells to achieve second harmonic suppression only ($2f_0$, where f_0 is the design frequency). The reported FBW was 10% with an impressive area reduction of 72%. In [19], similar specifications of harmonic suppression (up to $2f_0$ only), FBW (about 13%) and size reduction (73.2%) were achieved by employing interdigitated shunt capacitor with high-impedance TL. Harmonic suppression was improved to $3f_0$ in [20] by incorporating T-shaped micro-strip lines in place of λg/4 transformers. Compromise was made on the circuit area which was about 70.5% of the conventional BLC (29.5% area reduction) with an operating FBW of 10%. Another design with harmonic suppression up to $3f_0$ used meandered T-shaped TL technique [21] with an improved area reduction of 63.5% (owing to meandering of TLs). An improved out-of-band response up to $5f_0$ was achieved by using two shunt open stubs separated by a TL (π-shape) in [22] at the cost of more circuit area (37% size reduction) and narrow FBW (8%). The situation was improved in [23] where a unit consisting of a TL and triple stub was proposed to achieve harmonic suppression up to $6f_0$. Reported size reduction rate in [23] was 44% with a narrow operational FBW of 9%. In [24] a very wide out-of-band response up to $10f_0$ was reported by employing a triangular dumbbell shaped DGS scheme. Circuit area was significantly reduced to 65% at the cost of narrow FBW of about 8%. In a recently reported work exploiting modified T-shaped TLs [25], remarkable size reduction of 74% was achieved with harmonic suppression up to $8f_0$. The FBW however was less than 14.4%. Stepped impedance (low-high impedance) TLs were used to replace λg/4 transformers in [26]. More specifically, the low-Z high-Z low-Z (where Z stands for impedance) micro-strip structure shown in Fig. 1 (a) with impedance ratio $M > 1$ (where $M = Z_2/Z_1$), was used in the place of the vertical λg/4 transformers of the conventional BLC, whereas high-Z low-Z high-Z structure shown in Fig. 1 (b) with $M < 1$, was integrated horizontally. Using this technique, an area reduction of 50% was reported but the harmonic suppression was merely up to $2f_0$. From the above discussion, the fact stands out that for BLC design, there has been a trade-off between parameters like harmonic suppression, FBW and circuit area.

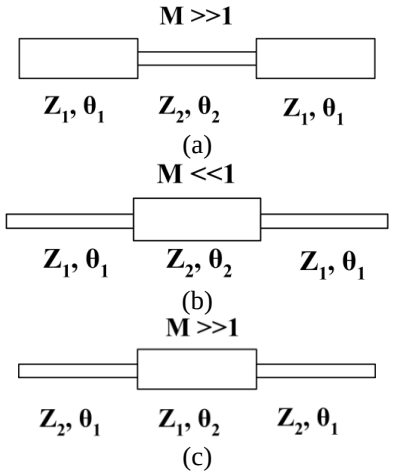

Fig. 1. Stepped impedance structures: (a) Conventional low-Z high-Z low-Z structure with $M > 1$, (b) conventional high-Z low-Z high-Z structure with $M < 1$, and (c) proposed high-Z low-Z high-Z structure with interchanged impedances and $M >> 1$.

In this paper we propose an unorthodox approach of analytically solving the structure in Fig. 1 (a) with a proposed length constraint ($2\theta_1 + \theta_2 = 45°$, for size reduction), to calculate low-Z (Z_1) and high-Z (Z_2) and interchanging them resulting in structure given in Fig. 1 (c), enforcing the condition $M (Z_2/Z_1) >> 1$ on the high-Z low-Z high-Z (stepped impedance sections of electrical length θ_1, θ_2, θ_1 respectively) structure. Please note here that the electrical length of the respective sections is kept the same as in Fig. 1 (a). The proposed methodology gives a superior out-of-band response as compared to that implemented in [26]. The primary reason behind an excellent harmonic suppression is a high M which ensures a transmission response (S_{21}) of HBLC approaching that of an ideal low pass filter (LPF) response [3]. This argument is based on the rationale given in section 2. The proposed structure shown in Fig. 1 (c) has an additional advantage of easier integration in 2-dimensions (2-D, vertical and horizontal arms) of the BLC primarily due to high-Z section with relatively thin width at the beginning. The proposed analytical solution results in high impedance ratio over a wide range of electrical lengths subsequently resulting in a wide range of high and low impedances (Z_2 and Z_1) to achieve good performance parameters. The designed HBLC based on proposed technique at a center frequency of 1 GHz,

achieved excellent harmonic suppression up to $9f_0$, an area reduction of 56% and a reasonable operational FBW of 30%.

II. ANALYSIS OF PROPOSED TECHNIQUE

Stepped impedance TL comprising of low-Z high-Z low-Z structure with an electrical length of θ_1, θ_2, θ_1 respectively as depicted in Fig. 1 (a) is adopted and analyzed first for evaluation and calculation of the impedances (Z_1 and Z_2) and respective electrical lengths. Subsequently by interchanging the Z_1 and Z_2 segments the structure is transformed to high-Z low-Z high-Z as shown in Fig. 1 (c) (enforcing M >> 1), which ultimately is integrated in place of horizontal 35Ω TL and vertical 50Ω TL (in 2-D) of the conventional HBLC. The effectiveness of this methodology, particularly in harmonics suppression is explained through comparison of the structures of Figs. 1 (a) and (c) later in this section.

Since the low-Z high-Z low-Z structure of Fig. 1 (a) can be considered as cascaded TLs, 2-port network analysis is applicable. In order to effectively replace conventional BLC TL of $\pi/2$ length (quarter wavelength) and impedance of Z_0, the equivalent ABCD parameters of this structure are kept equal to the ABCD parameters of the conventional BLC TL as given in Equation (1):

$$\begin{pmatrix} \cos\theta_1 & jZ_1\sin\theta_1 \\ \frac{j\sin\theta_1}{Z_1} & \cos\theta_1 \end{pmatrix}\begin{pmatrix} \cos\theta_2 & jZ_2\sin\theta_2 \\ \frac{j\sin\theta_2}{Z_2} & \cos\theta_2 \end{pmatrix}\begin{pmatrix} \cos\theta_1 & jZ_1\sin\theta_1 \\ \frac{j\sin\theta_1}{Z_1} & \cos\theta_1 \end{pmatrix} = \begin{pmatrix} 0 & jZ_0 \\ \frac{j}{Z_0} & 0 \end{pmatrix}_{\text{Conventional BLC}}, \tag{1}$$

Form Equation (1) it can be easily found that A = D and is given in Equation (2):

$$A = \cos\theta_1\cos\theta_2 - (M + M^{-1})\cos\theta_1\sin\theta_1\sin\theta_2, \tag{2}$$

Where $M = Z_2/Z_1$ is the impedance ratio. Putting A=0 and after some algebraic manipulations, M and M-1 can be given as:

$$\begin{aligned} M &= a + \sqrt{a^2 - 1} \\ M^{-1} &= a - \sqrt{a^2 - 1}, \end{aligned} \tag{3}$$

Where,

$$a = 0.5 \times \sec\theta_1 \cot\theta_1 \cot\theta_2.$$

Similarly, B parameter derived from (1) can be equated to jZ_0 to get an analytical equation for Z_1 as presented in Equations (4-5):

$$\begin{aligned} B &= jZ_1(2\cos\theta_1\cos\theta_2\sin\theta_1 + M\cos^2\theta_1\sin\theta_2 - M^{-1}\sin^2\theta_1\sin\theta_2) \\ &= jZ_0, \end{aligned} \tag{4}$$

Therefore,

$$Z_1 = Z_0 / [(2\times\cos\theta_1\cos\theta_2\sin\theta_1) + (M\cos^2\theta_1 - M^{-1}\sin^2\theta_1)\sin\theta_2)]. \tag{5}$$

It is worth mentioning here that Z_0 in Equation (5) is 35Ω and 50Ω for horizontal and vertical quarter wavelength TL of the conventional BLC respectively. It may also be noted here that Z_2 can either be calculated from C parameter derived from Equation (1) or directly from M once Z_1 is known, we use the latter calculation of Z_2. In order to solve Equations (3) and (5) to get M (and M^{-1}) and Z_1, a length constraint is introduced in Equation (6), which also serves as a means for miniaturization of the proposed HBLC:

$$2\theta_1 + \theta_2 = 45^\circ. \tag{6}$$

At this point Equation (3) coupled with Equation (6) is solved and the impedance ratio and its inverse is plotted in Fig. 2 (a) against θ_1 and θ_2. Subsequently, Equation (5) is solved for the calculated values of M (and M^{-1}), θ_1 & θ_2 and the curves for Z_1 and Z_2 (Z_2 obtained from $M = Z_2/Z_1$) for both 35Ω and 50Ω TL are plotted in Fig. 2 (b). It is imperative to note that the shaded area in Figs. 2 (a) & (b) indicates the practically implementable limits of M (M^{-1}), Z_1 and Z_2. Two primary parameters of concern in defining these bounds are Z_1 and M. The lower bound is set by considering Z_1 (for $Z_0 = 35\Omega$) such that its value should not be too low which translates into a very wide width of TL which may not be practically implementable. On the other hand upper bound is determined from M such that its value should not be too high which translates into a very high Z_2 (considered for $Z_0 = 50\Omega$) indicating a very thin TL which may not be fabricated by the machine (the machining lower limit in most cases is 0.1mm). Fine tuning of the layout circuit with or without meandering/mitering may be required for compact size.

The 'bath tub' like curve of M shown in Fig. 2 (a) depicts clearly that in the workable range (shaded area), M is greater than 10, fairly flat and ensures the condition of M >> 1 in the impedance interchanged structure of Fig. 1 (c) over a wide range of θ_1 & θ_2. It gives the designer a leverage of selecting suitable lengths θ_1 & θ_2 with a high M causing the transmission response (S_{21}) of proposed high-Z low-Z high-Z structure (with interchanged Z_1 and Z_2) shown in Fig. 1 (c) to follow that of an ideal LPF giving a good harmonic suppression. To prove this hypothesis, a comparison of S_{21} response of conventional structure in Fig. 1 (a) and proposed structure in Fig. 1 (c) is drawn in Fig. 3, for $\theta_1 = 14°$, $\theta_2 = 17°$, M = 13.5, $Z_1 = 8.42\Omega$, $Z_2 = 113.25\Omega$ (Z_1 and Z_2 selected for 35Ω TL from Fig. 2 (b)).

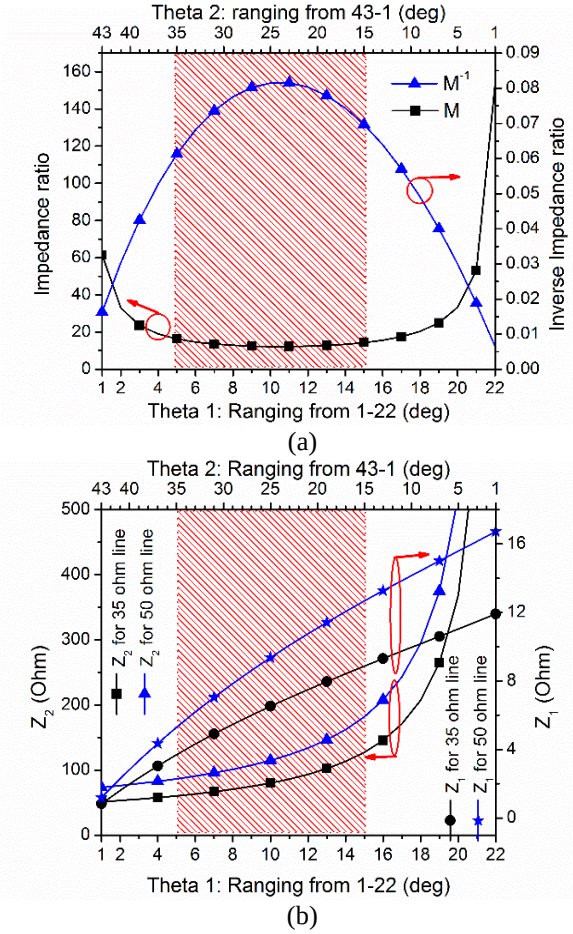

Fig. 2. Design graphs based on analytical solution: (a) Impedance ratio and its inverse, M (& M^{-1}) against wide range of θ_1 & θ_2, and (b) Z_1 and Z_2 for structure in Fig. 1 (a) against θ_1 & θ_2.

The simulation is carried out in Agilent's Advanced Design System (ADS) considering a 0.8mm thick substrate with dielectric constant of 2.2. It is very clearly shown in Fig. 3 that for a tuned response at 1 GHz, the proposed structure promises a good out-of-band performance as compared to the conventional structure. Very similar response can be simulated for structure replacing the 50Ω vertical branch of conventional BLC. It may be noted that Fig. 3 presents simulated response of just horizontal arm to prove the point. Actual response of the complete circuit may be different as shown subsequently.

The proposed high-Z low-Z high-Z structure (with M >> 1) is ultimately integrated in 2-D to get the schematic of the proposed HBLC as shown in Fig. 4. The design steps are stipulated as: 1) select suitable electrical lengths θ_1& θ_2 (such that the condition $2\theta_1 + \theta_2 = 45°$ is satisfied), 2) from Fig. 2 (a) get M (& M-1), 3) get the value of Z_2 and Z_1 for 35Ω and 50Ω TLs respectively from Fig. 2 (b), 4) calculate the widths corresponding to Z_1 and Z_2, 5) layout as per Fig. 4 by interchanging Z_1 and Z_2 (low-Z high-Z sections) and optimize.

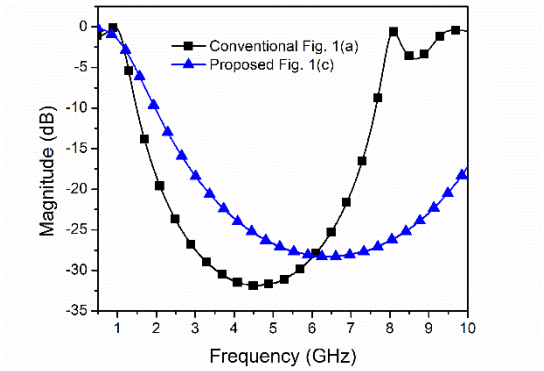

Fig. 3. Comparison of transmission coefficient (S_{21}) of structure in Fig. 1 (a) and proposed structure in Fig. 1 (c).

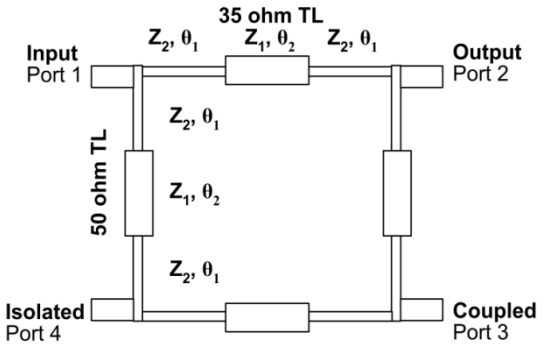

Fig. 4. Schematic of HBLC with proposed structure integrated in 2-D (not drawn to scale).

III. EXPERIMENTAL VERIFICATION

In order to validate the proposed technique, a hybrid branch line coupler was designed at 1 GHz and simulated in ADS. The designed HBLC was subsequently fabricated on a F4BM-2 substrate with dielectric constant of 2.2 and thickness of 0.8mm. For the purpose, the proposed high-Z low-Z high-Z structure was designed by: 1) selecting $\theta_1 = 14°$, $\theta_2 = 17°$, 2) M = 13.5, $M^{-1} = 0.074$, 3) for 35Ω TL, Z_2 = 113.25Ω, Z_1 = 8.42Ω; for 50Ω TL Z_2 = 162Ω, Z_1 = 12Ω, 4) for 35Ω TL, w_2 = 0.51mm, w_1 = 21.9mm; for 50Ω TL w_2 = 0.16mm, w_1 = 14.8mm, 5) with all these parameters known, the proposed high-Z low-Z high-Z structure was integrated in 2-D of the conventional BLC as per Fig. 4. The final layout of the designed HBLC was simulated. Some optimization, mainly mitering of low Z (Z_1) TL section of both 35Ω and 50Ω lines at an angle of 30°, and adjustment of width (within 4-6% of the original value) was carried out. Since the discontinuity between the High Z (less width) and Low Z (more width) TL section is bigger due to high M, slight adjustment of the width may optimize the results.

Fabricated HBLC at 1 GHz is depicted in Fig. 5.

Size of the proposed HBLC is reported to be 3.3cm × 3.9cm (or 0.15λg × 0.18λg). The achieved area reduction as compared to conventional BLC (with dimensions of 5.39 cm × 5.4 cm) at 1 GHz was 56%.

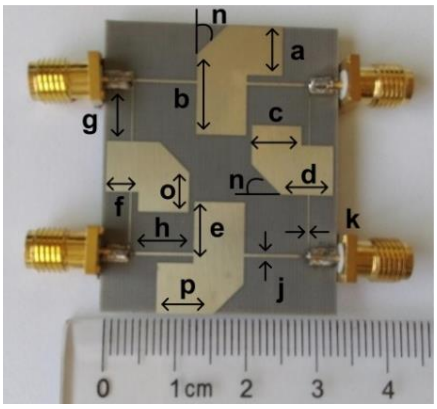

Fig. 5. Fabricated HBLC with proposed methodology. Dimensions (mm): a=7, b=11.3, c=7, d=7.3, e=8.5, f=4.35, g=7.2, h=8.82, j=0.41, k=0.16, o=5.5, p=7.8 and n=30°.

A. Results and discussions

All subsequent measurements were performed on Agilent's Microwave Network Analyzer model no. E8363B. Figure 6 (a) shows excellent conformance between the measured and simulated response of reflection (S_{11}) and transmission (S_{21}) coefficients of the designed HBLC. Measured return loss and insertion loss at port 1 stand at 29 dB and 3.5 dB respectively at 1 GHz. For S_{11} the measured 10 dB and 20 dB FBW is 29.4% (0.916 GHz – 1.21 GHz) and 13% (0.99 GHz – 1.2 GHz) respectively. For S_{21}, 1 dB FBW is reported to be 30% (0.94 GHz – 1.23 GHz). In addition, a very good out-of-band performance can be observed. The harmonic suppression of better that 15.5 dB is achieved up to $9f_0$. Insertion loss at port 3 (S_{31}), isolation between output ports 2 & 3 (S_{23}) and isolation at port 4 (S_{41}) are depicted in Fig. 6(b). Here too, almost overlapping simulated and measured responses can be observed. At 1 GHz, S_{31} = 3.02 dB and S_{23} = S_{41} = 29.7 dB indicating excellent power division, and isolation (both between the output ports 2 & 3 and isolated port 4). Achieved 1 dB FBW of S_{31} is 40% (0.76 GHz – 1.16 GHz) whereas 10 dB and 20 dB FBW of each of S_{23} and $S_{41}$are reported to be 33% (0.86 GHz – 1.16 GHz) and 11% (0.98 GHz – 1.09 GHz) respectively. S_{31} (transmission coefficient) exhibits an excellent harmonic suppression of better than 19.8 dB whereas out-of-band response of S_{23} and S_{41} is better than 15.5 dB till $9f_0$. Lastly, Fig. 7 shows the amplitude imbalance/difference ($|S_{21}| - |S_{31}|$) and phase imbalance/difference ($\angle S_{21} - \angle S_{31}$) between the signals at output ports. At 1 GHz, measured value of amplitude difference is 0.48 dB (less than ± 0.5dB), which can be verified from the inset graph of S_{21} and S_{31} in Fig. 7. The phase difference is 87.9° (which is within 90° ± 5°).

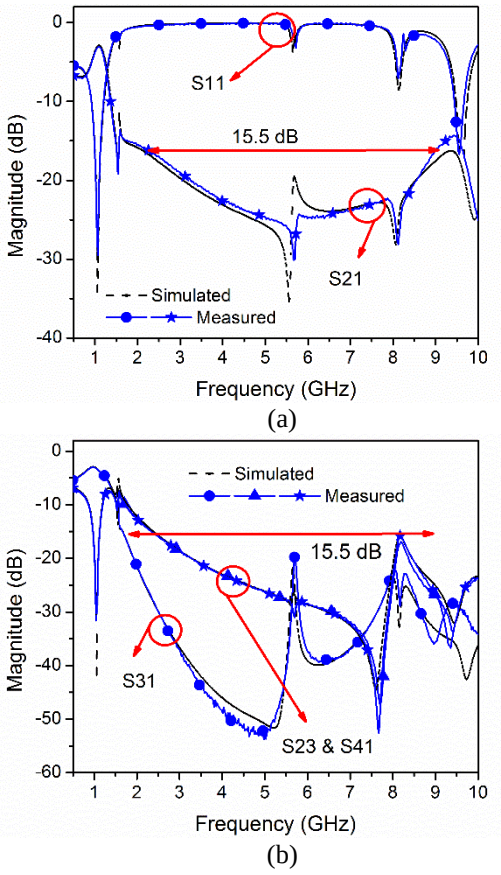

Fig. 6. Simulated and measured S-parameters response: (a) Reflection coefficient (S_{11}) at input port 1 and Transmission coefficient (S_{21}) at port 2, and (b) Transmission coefficient (S_{31}) at port 3, output port isolation (S_{23}) and isolation at port 4 (S_{41}).

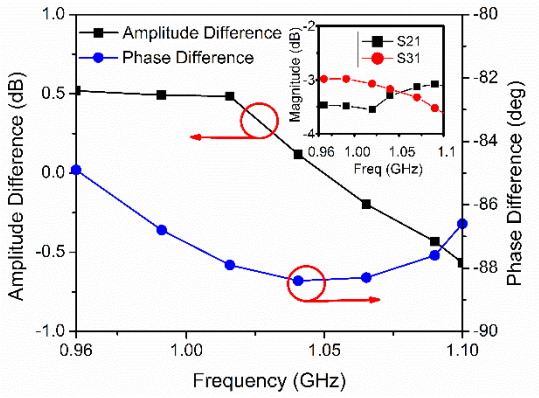

Fig. 7. Amplitude and phase difference of the signal at the output ports of the design HBLC.

B. Comparison with previous works

A candid comparison of the proposed design with already published work is presented in Table 1.The main focus is comparison of three design parameters namely FBW, circuit size reduction (as compared to the conventional BLC) and harmonic suppression. It can be clearly seen in Table 1 that [8 – 12] offer a size reduction rate of up to 50% and FBW of up to 32% but with no harmonic suppression, while [13 – 17] give superior area reduction of up to 63% and a wider FBW at the cost of out-of-band performance. From the works reporting good out-of-band performance [18 – 25], it can be inferred that a relatively narrow FBW was achieved although area reduction in some cases have been phenomenal (> 60%) [18],[19],[24],[25].

Our proposed design, although achieved a size reduction of 56%, promises wider FBW of about 30% with a superior harmonic suppression up to $9f_0$ (except for [24] where harmonic suppression is $10f_0$ but FBW is very narrow). Another important thing to note is that the proposed technique of utilizing the stepped impedance TL gives much better results as compared to similar structure used in [26].

Table 1: Comparison of proposed work with literature

Ref.	Freq. (GHz)	Circuit Configuration	FBW[a] (%)	Size Reduction	Harmonic Suppression
[8]	2.4	DGS	10	33	No
[9]	0.9	Cascaded TL with centrally loaded open stub	10	55	No
[10]	1.94	Comb line structure	23	22.6	No
[11]	2.4	Asymmetrical T-shaped structure	~24	55	No
[12][b]	1.8	Polar Curves	32	50	No
[13]	1.5	Substrate integrated suspended line (SISL) technology	21	62	No
[14]	1	Cascaded slow-wave cells	32	62	No
[15]	2.4	Combination of dual TL & π-model	40	47	No
[16]	2.4	Dual TL	43	63.9	No
[17]	2.4	π-model artificial TL	33	62	No
[18]	2	Slow-wave resonant cells	10	72	Up to $2f_0$
[19]	0.836	High impedance TL with interdigitated capacitance	<13	73.2	Up to $2f_0$
[20]	2	T-shaped structure	10	29.5	Up to $3f_0$
[21][b]	2.1	Meandered T-shaped structure	Not given	63.5	Up to $3f_0$
[22]	0.5	π-shaped structure	8	37	Up to $5f_0$
[23]	1	TL with triple stub	9	44	Up to $6f_0$
[24]	1	DGS	<8	65	Up to $10f_0$
[25]	0.9	Modified T-shaped structure	<15	74	Up to $8f_0$
[26]	1	Stepped impedance TL	Not given	50	Up to $2f_0$
This work	**1**	**Stepped Impedance TL**	**30**	**56**	**Up to $9f_0$**

[a] 10 dB fractional bandwidth.
[b] only BLC results have been quoted.

IV. CONCLUSION

A novel technique of utilizing the stepped impedance TL structure is presented for the design of HBLC in micro-strip technology. First of all conventional low-Z high-Z low-Z structure is analysed by imposing a length constraint. After finding out the impedance of each section, they are interchanged to form a high-Z low-Z high-Z structure of Fig. 1 (c) ensuring impedance ratio, M (Z_2/Z_1) >> 1. Owing to high impedance ratio (M) over a wide range of electrical lengths, the transmission coefficient (S_{21} and S_{31}) response follows that of an ideal LPF promising wide range of harmonic suppression. The proposed theory is practically verified by fabricating an HBLC at 1 GHz. An excellent harmonic suppression of up to $9f_0$ was achieved with an operational FBW of 30% and size reduction of 56%. In short, the proposed HBLC is easy to fabricate, has no lumped elements and is compact enough to fulfill the requirements of bandwidth

hungry micro-wave systems requiring wide harmonic suppression.

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