# IMPATT Efficiency Extraction Using On-Chip Antenna Radiation

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***Abstract*****—IMPATT diodes were designed and integrated with microstrip patch antenna on–chip in standard CMOS technology to extract the efficiency beyond avalanche frequency. By comparing the on-chip simulations and measurements of an IMPATT diode integrated in a CPW to an integrated one with a microstrip patch antenna at the same biasing conditions, the results demonstrated an efficiency ranging from ~ 0.01% to 0.016% without and with the added surface roughness losses, respectively. Such variation is strongly associated with the uncertainty provided by the increase of conduction losses ranging between 40%~80% beyond the avalanche frequency.**

**Keywords—*avalanche frequency, coplanar waveguide, high frequency, IMPATT diode, microstrip patch antenna, skin depth, surface roughness, transmission line.***

## I. INTRODUCTION

The demand for precise and robust on-chip efficiency measurements of (Impact Avalanche Transit Time) IMPATT diodes is increasing due to the recent developments in IMPATT-Antenna integration for monolithic millimeter-wave applications in standard CMOS technology [1]. This accuracy affects the design and the optimization of the oscillation frequency and the radiated power.

IMPATT diode is a solid state device that converts the DC power into RF one by generating negative resistance beyond avalanche frequency [2-3]. CMOS IMPATT diodes demonstrated the capabilities of generating avalanche frequency beyond 30 GHz and negative resistance up to 80GHz [1-5]. The generation of the negative resistance and the capacitive reactive part at frequencies beyond the avalanche frequency is affected by controlling the breakdown voltage and the operating current [1-5].

In this paper, we demonstrate a robust on-chip integration and extraction methodology for the IMPATT diode efficiency beyond avalanche frequency.

## II. THE ANTENNA INTEGRATION

The on-chip lateral IMPATT diodes have been monolithically integrated with microstrip patch antenna in standard CMOS technology and successfully de-embedded and characterized [1]. With such configuration, the antenna can serve as a resonator and radiator simultaneously.

Using a patch antenna driven by a lateral IMPATT diode, the 4 $mm^2$ transmitter was DC biased at 11V with measured current of 30mA (Fig. 1). The modeled antenna with different levels of generated and radiated power is shown in Fig. 2, while the measured power at the spectrum analyzer is -62dBm at 77GHz (Fig. 3). By using this particular configuration, area requirements and several antenna losses including dielectric, conduction [6], radiation, surface wave and surface roughness losses [7] of the integrated transmitter are reduced.

## III. RESULTS AND DISCUSSION

The test setup includes an Anritsu ME7220A Radar Test System (RTS), WR12 E-band horn Antenna, and MS2663C 9K-8.1GHz spectrum analyzer (Fig. 3). The frequency band of the transmitter is initially down-converted by the RTS from 76-77GHz to an IF band of 4.7-5.7GHz before the radiated signal is characterized [1].

Initially, the supply is maintained at zero volts, and slowly increased (to avoid any surges), up to the operating voltage of the diode. At the nominal breakdown voltage of ~10V, a current of 2mA flows. As the supply voltage is gradually increased, the current drawn by the circuit also increases. When the on-chip transmitter is biased at 11V, the corresponding quiescent current is 30mA, and a signal is detected with an oscillation frequency of 77GHz, as shown in Fig. 3.

The Sonnet simulated results for the Directivity and the Gain of the patch antenna are 11dB and -23dB, respectively (Fig. 4). Once the surface roughness factor is included the Gain drops to -26dB. This indicates that the total losses of the antenna are 34dB and 37dB without and with the surface roughness impact, respectively. More simulated results are summarized in Table I for different dielectric thickness. It is clear that the dielectric thickness, is our main contributor to the low radiated power and the large simulated losses.

Based on the measured radiated power, the system losses, and the shift of the avalanche frequency [6-8], the calculated diode efficiency ranges between – 38dB to -41dB. This low efficiency is largely a result of the high capacitive loading from the depletion region [9]. Table II summarizes the generated and the radiated power at different stages.

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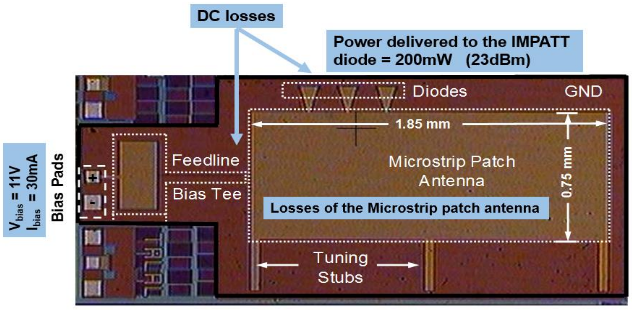


Fig. 1. Die photo of integrated IMPATT diode with microstrip patch antenna on-chip [1].

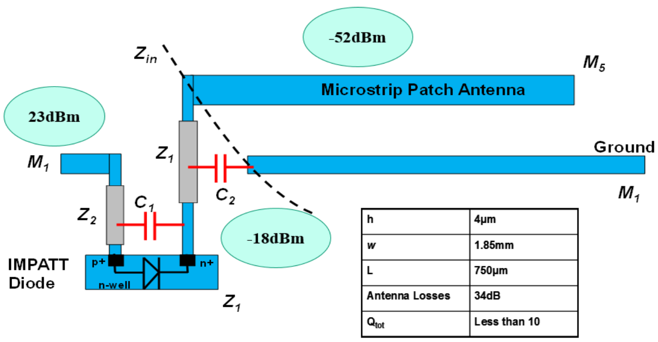


Fig. 2. The modeled antenna with the different power levels (the case with excluded surface roughness [7]).

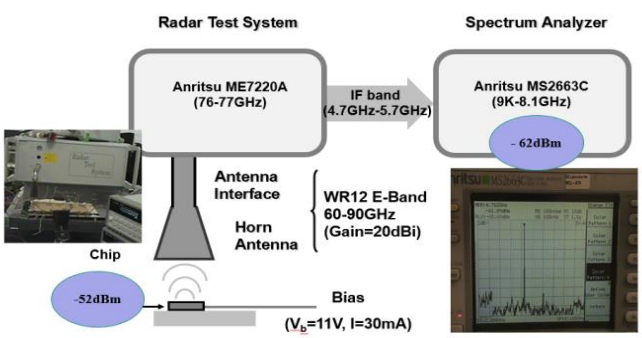


Fig. 3. Measurement setup, which includes Anritsu ME7220A Radar Test System (RTS), WR12 E-band horn Antenna, and Anritsu MS2663C 9K-8.1GHz spectrum analyzer.

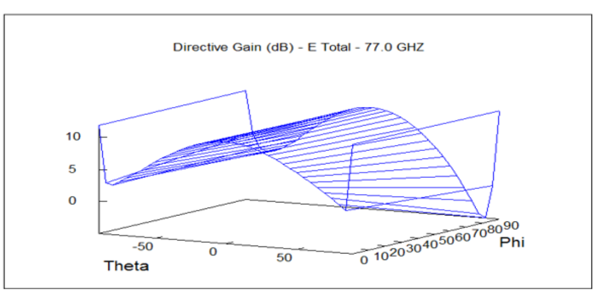


Fig. 4. The simulated directive gain of the CMOS microstrip patch antenna using Sonnet.

Table I: Simulated losses of on-chip antenna with different dielctric thickness (exluding the surface roughness) [7]

| Dielectric Thickness (h) (µm) | Total Losses (dB) |
|---|---|
| 100 | 8 |
| 30 | 14 |
| 10 | 20 |
| 4 | 34 |

Table II: Power measured at different levels with extracted IMPATT effeciency

| | |
|---|---|
| DC power delivered to the transmitter | 330mW (25dBm) |
| DC losses including: | 2dB |
| Power delivered to the IMPATT diode | 200mW (23dBm) |
| Losses of the Microstrip patch antenna: (Without Surface Roughness) (With Surface Roughness) | 34dB 37dB |
| Losses of the measurement setup (from the horn antenna to the spectrum analyzer) | 10dB |
| Calculated power generated by the diode (Without Surface Roughness) (With Surface Roughness) | -18dBm -15dBm |
| Extracted diode efficiency (First lateral IMPATT efficiency 0.03% (-35dB) [9] ) (Without Surface Roughness) (With Surface Roughness) | -41dB (0.01%) -38dB (0.016%) |

## IV. Conclusion

The realized integration of IMPATT diodes and on-chip microstrip patch antenna demonstrated considerable changes in the extracted IMPATT efficiency beyond avalanche frequency. This paper revealed the robustness of the methodology proposed despite the present impact of the surface roughness on the IMPATT efficiency. Based on the measured radiated power and the system losses, the extracted diode efficiency is ranging between -41dB to -38dB without and with the surface roughness, respectively. Because of the cost-efficiency and the robustness of standard CMOS manufacturing, this type of monolithic integrated transmitter may be well suited for use in IMPATT diode efficiency extraction beyond avalanche frequency.

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