An X-Band GaN HEMT Oscillator with Four-Path Inductors

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Abstract ─ An X-band GaN HEMT oscillator implemented with the WIN 0.25 μm GaN HEMT technology is proposed. The oscillator consists of a HEMT amplifier with an LC feedback network with four-path inductors. With the supply voltage of V_{DD} = 2 V, the GaN VCO current and power consumption of the oscillator are 10.8 mA and 21.6mW, respectively. The oscillator can generate single-ended signal at 8.82 GHz and it also supplies output power 1.24 dBm. At 1MHz frequency offset from the carrier the phase noise is 124.95 dBc/Hz. The die area of the GaN HEMT oscillator is 2×1 mm^2.

Index Terms ─ 0.25 μm GaN HEMT, LC oscillator, output power, phase noise.

I. INTRODUCTION

Gallium Nitride (GaN) High Electron-Mobility Transistor (HEMT) devices with high carrier mobility and high breakdown voltage are of great interest because of their suitability for high power RF applications and power switches [1-3]. A GaN power amplifier, if monolithically integrated with a low phase-noise oscillator can provide a flexible high-power signal source, and GaN oscillators are thus indispensable in fully integrated GaN HEMT transceivers. A few GaN HEMT oscillators have been presented in the past. Colpitts oscillator [1]-[3] uses one HEMT and a stub or inductor between the HEMT's source and the ground, providing a positive series feedback to make the HEMT VCO unstable. The second HEMT oscillator uses the common-gate topology with a feedback transmission line element at gate to maximize the device instability [4]-[5]. The resonator circuit is placed at the HEMT device's source side to compensate the opposite sign of reactance from the un-stabilized common-gate device. The third HEMT oscillator uses Hartley topology [6], the source of GaN HMET is grounded. Differential GaN HEMT oscillators [7] are convenient to connect directly to a differential input. The common gate balanced Colpitts oscillator [8]-[10] provides differential outputs and is chosen since it is known for low up-conversion of flicker noise. The above-mentioned oscillators use single-path inductors. This letter presents a GaN oscillator with four-path inductors. Multi-path inductors have been shown to have high-quality factor [11], and are potential for resonator usage and for low phase noise oscillator design. The designed GaN oscillator was manutured with a 0.25 μm GaN on SiC foundry process technology [12].

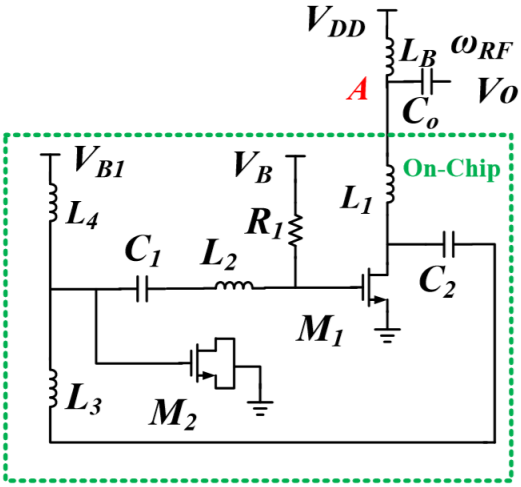

Fig. 1. Schematic of the presented oscillator.

II. DETAIL CIRCUITS DESIGNS

Figure 1 shows the schematic of the designed GaN HEMT oscillator. The oscillator uses an active HEMT, air-bridge interconnects, spiral planar inductors, and metal–insulator–metal (MIM) capacitors. The circuit was designed using Agilent Technologies' Advanced Design System (ADS). The inductor L_1 and HEMT M_1 forms an amplifier and R_1 is gate-biasing resistor. V_B is the gate voltage. V_{DD} is the supply voltage and is connected to the output node A through an RF choke L_B. C_1, C_2 are dc blocking capacitors. HEMT M_2 is used as varactor. V_{B1} is the varactor control voltage using an RF bias inductor L_4. The output is measured at the common node A of L_1 and RF choke. L_3 is used to adjust oscillation frequency and improve the phase noise.

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Inductor L_2, gate-source capacitor of HEMT M_1 and varactor M_2 forms a resonator. L_3 and L_2 are four-path inductors. Inductor L_4 is a symmetric single-path spiral inductor. For simplicity of design guide, authors short A node to the ground, and eliminate M_2 and L_4.

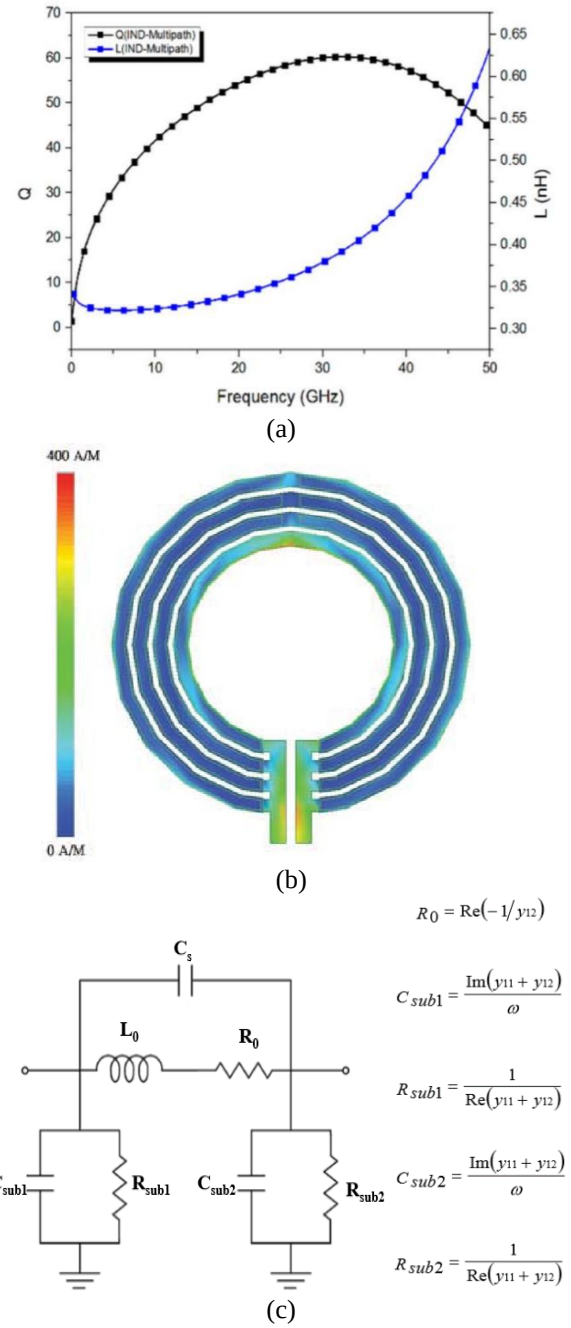

Fig. 2. (a) Chip micrograph for the HEMT oscillator; 2mm×1mm. (b) Simulated current density, simulated *L* and *Q* characteristics of the designed 4-path inductor. (c) A lumped physical model of a circular inductor.

The small-signal model for the oscillator can be built to derive the resonant frequency given by:

$$\omega = \sqrt{\frac{1}{[L_2 + L_3 + L_1]C_{gs}}}. \quad (1)$$

And the equivalent negative resistance used for the resonator is given by:

$$-\mathrm{R} = -\frac{1 - \mathrm{L}_1[\omega^2[L_2 + L_3]\mathrm{C}_{gs}}{\mathrm{g}_m}. \quad (2)$$

Using Leeson's equation as shown in (3), the estimated phase noise improvement is 15 dBc/Hz due to the Q-factor improvement:

$$L(f_m) = 10\log\left[\frac{1}{2}\left(\left(\frac{f_o}{2Q_1 f_m}\right)^2 + 1\right)\left(\frac{f_c}{f_m} + 1\right)\left(\frac{FkT}{P_s}\right)\right]. \quad (3)$$

This article proposes that silicon-on-sapphire (SOS) and micro-electro-mechanical system (MEMS) technologies can be used to proposed high Q-factor inductors operating in X-band. Cgs is the gate-source capacitance and gm is the transconductance of HEMT M_1. –R is used to compensate the loss in the passives and output. Varying V_B to change Cgs is used to tune the oscillation frequency. Figure 2 shows simulated inductance L and Q characteristics of the 4-path L_2 as shown in Fig. 1. Three path inductors have been used previously for low phase noise silicon-based oscillator design [13]. The inductance and quality-factor are extracted from the y parameter. At 10 GHz, the Q-factor is 40 for the designed inductor with L=0.325nH. The self-resonant frequency is about 65 GHz. Figure 2 (c) illustrates the lumped physical model proposed for these suspended inductors. L_0 and R_0 are series inductance and resistance due to conductor losses and dissipation from the induced eddy currents in the substrate. Cs is an inter-turn fringing capacitance and a metal overlap coupling capacitance between the spiral and underpass metal layers. In addition, R_{sub} and C_{sub} are the resistance and parasitic capacitance of the substrate. The inductors parameter of R_0, C_{sub}, R_{sub} and Q-factor are modelled using equations (4). After calculation from equations (4), optimized values of each lump elements determined L_1~L_4 and C_0~C_2 depended on Fig. 2 (c) equivalent circuit in Fig. 1:

$$Q_{factor} = \frac{\omega L_0}{R_0} \cdot \frac{R_{sub}}{R_{sub} + \left[\left(\frac{\omega L_0}{R_0}\right)^2 + 1\right]R_0} \cdot \left[1 - \frac{R_0^2(C_s + C_{sub})}{L_0} - \omega^2 L_0(C_s + C_{sub})\right]$$

$$Q_{factor} = \frac{\mathrm{Im}\left(\frac{1}{y_{11}}\right)}{\mathrm{Re}\left(\frac{1}{y_{11}}\right)}. \quad (4)$$

III. EXPERIMENTALS

The VCOs were designed and fabricated in the WIN 0.25 μm GaN/SiC HEMT process base on simulated and numerical modeling. Figure 3 shows the micrograph of the proposed oscillator with a chip dimension of 2×1 mm^2 including all test pads and dummy metal. Figure 4 shows the measured output voltage waveform of the oscillator. It shows low high-order harmonic. Figure 5 shows the measured output spectrum of the fundamental signal at 8.82 GHz with output power 1.24 dBm. At V_{DD}=2V, the power consumption is 21.6 mW. Figure 6 shows the phase noise performance of VCO. The measured phase noise of VCO is about -124.05 dBc/Hz at 1MHz offset frequency from 8.82 GHz oscillation frequency and has a slope of -30 dB/dec in the frequency offset below 1 kHz the phase noise consists of the $1/f^3$ portion and is due to the flicker noise [14]-[15]. The figure of merit. (FoM) has been defined in Eq. (5) to compare performances of VCOs.

$$FOM = L\{\Delta\omega\} + 10\cdot log(P_{DC}) - 20\cdot log\left(\frac{\omega_o}{\Delta\omega}\right), \qquad (5)$$

where ω_o is the oscillating frequency, $\Delta\omega$ is the offset frequency, $L\{\Delta\omega\}$ is the phase noise at $\Delta\omega$, PDC is DC power consumption of VCOs in mW. By the calculation, the FoM of the proposed VCO is -189.56 dBc/Hz. The FoM is calculated at 1MHz offset frequency and V_{DD}=2V. Figure 7 shows measured phase noise increased with V_{DD}. Increasing V_{DD} can increase voltage swing to enhance S/N ratio ideally, however, when V_{DD} is beyond 2V, this is not guaranteed because the phase noise increases with supply voltage [16]-[18]. Figure 8 shows measured power consumption, output power, and oscillation frequency versus V_B. Maximal output power is measured at V_B=-2.1V. Table 1 shows the performance parameters comparison of the designed GaN HEMT oscillators with others published articles.

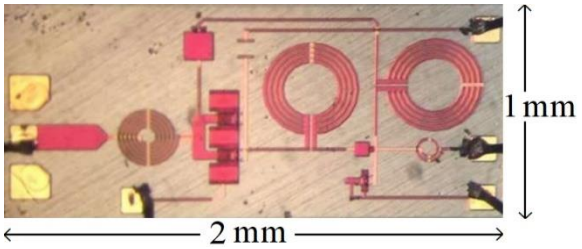

Fig. 3. Chip micrograph for the HEMT oscillator (chip area = 2mm×1mm).

Fig. 4. Measured voltage waveform. V_{DD}=1 V, V_{B1}=0 V, V_B=-2 V. L_{choke}=4.7nH.

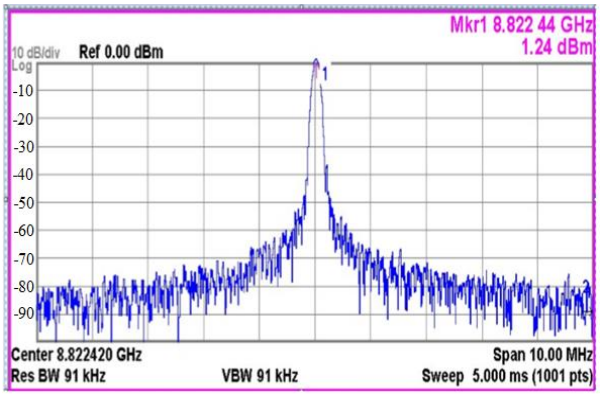

Fig. 5. Measured spectrum. V_{DD}=2V. V_B=-2.0V. V_{B1}=0V.

Fig. 6. Measured phase noise. V_{DD}=2V, V_{B1}=0V, V_B=2V. L_{choke}=4.7nH. A $1/f^3$ guideline is used for reference.

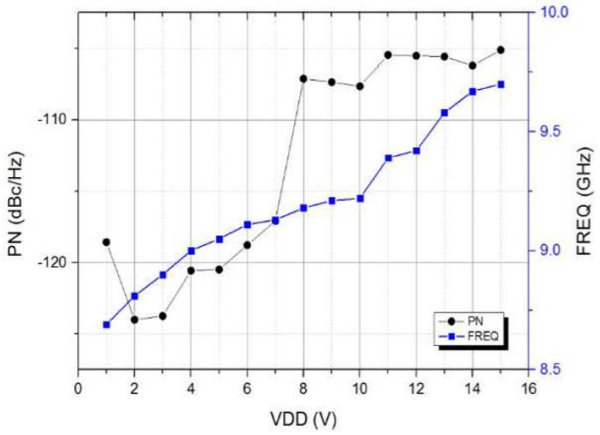

Fig. 7 Measured phase noise and oscillation frequency versus V_{DD}. V_{B1}=-2V. V_T=0 V.

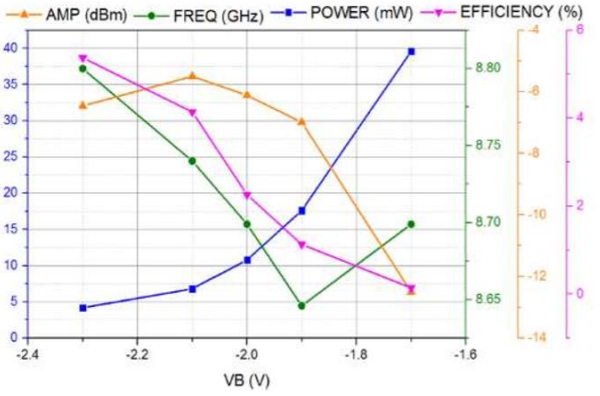

Fig. 8. Measured power consumption, output power, and oscillation frequency versus V_B. V_{DD}=1V. V_{B1}=-2.3~1.7V.

Table 1: Performance comparison of GaN VCOs

Ref.	Proc. (um)	Topol	Vdd(V)/ Pdis(mW)	fo GHz	PN dBc/Hz	FOM dBc/Hz
[10]	0.25	Hartley	28/1456	7.9	-112@ 100KHz	-178
[6]	0.25	Balanced Colpitts	6/180	9.92	-136	-193
[19]	-	Push-push	15/600	9.1	-130	-181
[20]	0.25	Common source	10/600	9.9	-135	-187
[5]	0.25	Common Gate	30/10625	9.55	-115.0	-154.0
This	0.25	Cross-coup	2/21.6	8.8	-124.05	-189.56

VI. CONCLUSION

A 8.8 GHz high power VCO using GaN HEMTs was designed, fabricated, and characterized. At the supply 2V, the output power of the carrier at 8.8 GHz is 1.24 dBm. The measured phase noise of VCO is about 124.05 dBc/Hz at 1MHz offset frequency from the carrier. The phase noise is mainly due to the device flicker current noise. At V_{DD}=2V, the oscillator can supply high output power and low phase noise with the FOM -189.56 dBc/Hz. The power conversion efficiency is 12%. To authors' knowledge, multi-path inductor has been successfully implemented in GaAs process for the first time in literature.

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