Crosstalk Reduction on Delay Line with Rectangular-Patches (RPs) Design

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Abstract ─ In this paper, a novel helix delay line with RPs structures is proposed to investigate the performance of crosstalk reduction. In the past, conventional delay lines consist of equal-length parallel unit lines which are closely packed to minimize the fabricated cost and routing area. All spacing between the adjacent parallel unit lines of delay lines should be smaller. When the operating signal frequency ups to the GHz level, the electromagnetic noise has become a dominant issue coupling from adjacent lines. It is called as a crosstalk source. The crosstalk may affect system-level timing. Besides, it causes error switching of logic gates that will reduce the signal quality. The feature of proposed helix delay line is that the far-end crosstalk (FEXT) is a dominated noise that accumulates at the receiving end. RPs structures are added and aligned at the center of the two parallel adjacent unit lines of the proposed helix delay line, which are used to reduce the difference between inductive and capacitive coupling coefficient ratios, and to reduce FEXT that maintains the signal integrity (SI) quality on receiving end.

Index Terms ─ Far-End Crosstalk (FEXT), helix delay lines, Rectangular-Patches (RPs), Signal Integrity (SI).

I. INTRODUCTION

Crosstalk is usually represented in terms of near-end crosstalk (NEXT) and FEXT [1]. FEXT is induced by the difference between the inductive coupling ratio and the capacitive coupling ratio. In addition, FEXT is also proportional to the length of parallel trace and exists in an inhomogeneous environment only, e.g., the microstrip geometry [2], [3]. In the past several years, the popular delay lines are with serpentine routing and spiral routings [4], [5]. In conventional serpentine and spiral delay lines, NEXT is a dominant noise that propagates to the receiving end. The noise accumulated at the receiving end will result in time-domain transmission (TDT) waveform degradation and affect the eye-diagram quality. Although there are many strategies for crosstalk noise reduction in early studies, the crosstalk noise such as NEXT always exists.

In order to reduce the NEXT and FEXT between adjacent parallel lines of the delay line, many design rules and techniques have been adopted by designers. A well-known 3W rule is a general method of reducing the crosstalk in which separation between adjacent lines of three times of line width [6]. A guard trace added within two adjacent lines is also a common method for crosstalk reduction. However, a guard trace without a terminator will experience noise and act as a potential source of noise for the victim [7], [8]. In contrast to the guard trace without termination, two terminators matching the line impedance can be placed on both ends of the guard trace to terminate the noise energy and reduce the crosstalk [9]. In the shorting-vias guard trace method [10], guard trace with grounded vias can maintain the stable grounded potential at every via point. In the via fences method [11], it is well known that a guard trace which is shorted at multiple points will lead to the lowest amount of crosstalk. It is because the via fence is designated to reduce the coupling between two adjacent lines. In order to reduce the crosstalk in parallel double microstrip lines, the optimal number and location of grounded vias method will be adapted for preventing the crosstalk as well [8]. In addition, a serpentine guard trace with the grounded vias was proposed to reduce the crosstalk between two adjacent parallel lines [12]. Besides, a new design of FEXT crosstalk reduction is proposed by using the rectangular-shape resonators on two parallel-coupled microstrip lines [13]. Nowadays, there are some studies for FEXT reduction such as using a homogeneous dielectric substrate on PCBs [14], coated graphene on microstrip lines [15], surface mount capacitors on FEXT mitigation [16], and RSR for FEXT mitigation [17]. However, using a homogenous dielectric substrate, graphene, and capacitor increases the PCB cost and probably increase the production loss.

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Based on the last studied in [18], some new investigations and extensions in FEXT reduction are shown in this paper. For example, the derivation on the section of the three-coupled lines is equivalent to the mathematical models of the mutual-capacitance. The design methodologies in determining the dimensions of RPs for increasing the mutual-capacitance between the adjacent parallel lines, and the representations of both three-coupled lines and two-coupled lines sections are concatenated together for FEXT calculation. This equation is presented in this paper.

This paper is organized as follows: a brief characterization of crosstalk is revisited in Section II. The proposed helix delay line and the crosstalk analysis are illustrated in Section III. In Section IV, we focus on the design methodology of determining the dimensions of RPs. In addition, equivalent capacitance circuit model of the three-coupled lines section, and the relationship between capacitance values and inductance values are also presented. The comparisons between the simulated and the measured results are presented in Section V. Some Brief conclusions are presented in Section VI. Finally, one RPs design example for increasing mutual-capacitance in two parallel adjacent unit lines was shown in the appendix section to improve the readability of this paper.

II. INTRODUCTION TO NEXT AND FEXT

Crosstalk occurs due to the coupling effects caused by the mutual-capacitance and the mutual inductance of the victim and aggressor lines, driven by the transient signals in the aggressor. The end of the victim closer to the driver (receiver) of the aggressor is called the near (far) end. When the rise and fall times of the aggressor's transient logic state change continuously, the signal operation of the victim will be destroyed because the energy coupling is transferred from the aggressor [1]. Crosstalk is usually represented in terms of NEXT and FEXT. The formulas for NEXT and FEXT can be represented as:

$$V_{NEXT} = \frac{V_{in}}{4}\left(\frac{L_m}{L_S} + \frac{C_m}{C_T}\right), \quad (1)$$

$$V_{FEXT} = \frac{-V_{in} \cdot TD}{2t_r}\left(\frac{L_m}{L_S} + \frac{C_m}{C_T}\right), \quad (2)$$

where V_{in} is the input voltage, TD is the time delay, t_r is the rising time, L_S is the self-inductance, L_m is the mutual-inductance, C_T is the self-capacitance, and C_m is the mutual-capacitance [19]. As can be seen from equation (2), the amplitude of FEXT is determined by the difference between the inductive coupling ratio (L_m/L_s) and the capacitive coupling ratio (C_m/C_T). For example, in some practice cases, the unit length of two adjacent parallel lines with microstrip geometry, where the dielectric constant of the surrounding air is less than that of the inside PCB dielectric constant, the inductive coupling ratio is always larger than the capacitive coupling ratio. Thus, FEXT is a negative pulse.

III. CROSSTALK IN HELIX DELAY LINE

The novel helix delay line without RPs structures and with RPs structures are shown in Fig. 1 (a) and Fig. 1 (b), respectively. In Fig. 1 (a), all unit lines (e.g., sections of A-C, C-D, etc.) in the helix delay line always keep counter-clockwise routing. Besides, it has the same width and spacing between adjacent unit lines that is used to maintain the impedance under the acceptable level. In addition, both the helix delay line without RPs and the helix delay line with RPs structures are employed with microstrip geometry. The via hole is used to connect the line between the top and the bottom layers at point R under the line impedance that maintains the acceptable level. The cross-sectional view is shown in Fig. 1 (c).

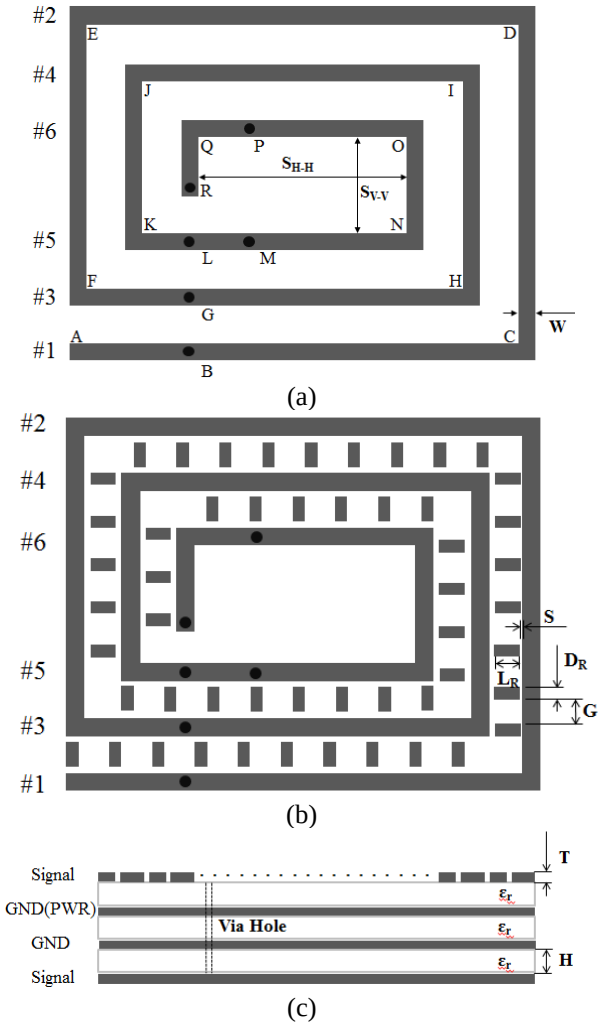

Fig. 1. The schemes of helix delay line. (a) without rectangular-patches (RPs); (b) with rectangular-patches (RPs); (c) the cross-sectional view.

Based on the assumption that the weak coupling condition was considered in the helix delay line, the noise induced on the adjacent victim line rarely affects

the main stimulus signal on the aggressor line [20], [21]. As can be seen in Fig. 1 (a), when a main stimulus step signal travels down all unit lines (i.e., point A to C, C to D, etc.) to the receiving end (i.e., point R) of the helix delay line, the crosstalk will be induced. The best two units are formed when two unit lines are in the nearest neighborhood to the main stimulus signal. E.g., when a main stimulus step signal propagates to point G of #3 unit line, meanwhile, crosstalk was induced on point B of #1 unit line and point L of #5 unit line. In point B of #1 unit line, the crosstalk is the result of the mutual capacitance in conjunction with the mutual inductance between adjacent unit lines. Thus, it can be divided into two directions. Due to the fact that this crosstalk observed on the adjacent unit lines (i.e., #1 unit line) far away from the driver end of point F, one crosstalk propagates to the point C of #1 unit line and it finally propagates to point R of receiving end. It is given by *FEXT* ($V_{far\text{-}end}$). Another one propagates to point A of #1 unit line. Because this crosstalk is close to the driver end of point F, it is given by *NEXT* ($V_{near\text{-}end}$). The same condition happens when a main step stimulus signal is at point G of #3 unit line. The crosstalk was induced on point L of #5 unit line and can divide it into two directions. One propagates to the point N of #5 unit line, given by *FEXT* ($V_{far\text{-}end}$). Another one propagates to point K of #5 unit line, given by *NEXT* ($V_{near\text{-}end}$). The FEXT on point B of #1 propagates to the receiving end of the helix delay line behind the main stimulus signal. On the contrary, the FEXT on point L of #5 propagates to receiving end of helix delay line ahead of the main stimulus signal.

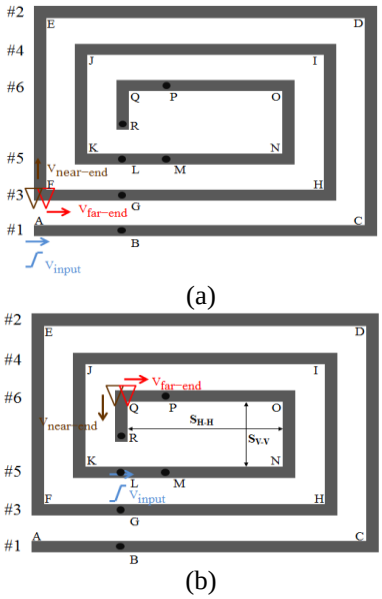

Fig. 2. The crosstalk on the helix delay line. (a) NEXT and FEXT on #3 unit line; (b) NEXT and FEXT on #6 unit line.

For a simple crosstalk analysis, let us consider the crosstalk that can be seen on all unit lines. It propagates to the receiving end ahead of the main stimulus signal when the main stimulus signal travels down all unit lines of the helix delay line. As can be seen in Fig. 2 (a), we consider a helix delay line with twelve unit lines. When a main stimulus step signal with amplitude (V_{input}) and rise time (t_r) was driven at point A of #1 unit line, crosstalk was induced at point F of #3 unit line and can divide into two parts. One is a FEXT at point F of #3 unit line. It propagates toward the point H of #3 unit line. This crosstalk finally propagates to the receiving end of point R. Another one is NEXT at point F of #3 unit line. It propagates toward the point E of #2 unit line. This crosstalk finally propagates to the driver end of point A. As can be seen in Fig. 2 (b), when a main stimulus step signal propagates to point L of #5 unit line, crosstalk current is induced at point Q of #6 unit line. Because the crosstalk is the result of the mutual capacitance in conjunction with the mutual inductance between adjacent unit lines, it can divide into two directions. One propagates to the point O of #6 unit line. Finally, this crosstalk propagates to point A of #1 unit line. Besides, this crosstalk is observed on the adjacent unit lines (i.e., #6 unit line) that is far away from the driver end when the main stimulus signal propagates along #5 unit line, given by *FEXT* ($V_{far\text{-}end}$). Another one is that it propagates to point R of receiving end. This crosstalk can be seen on the adjacent unit lines close to the driver end when the main stimulus signal propagates along #5 unit line, given by *NEXT* ($V_{near\text{-}end}$). The same analysis method can consider the crosstalk which can be seen on all unit lines and propagates to the receiving end behind the main stimulus signal.

All $V_{far\text{-}end}$ induced from adjacent unit lines will propagate to point R of receiving end when a main stimulus step signal travels down all unit lines from point A of #1 unit line to L of #5 unit line. On the other hand, in Fig. 2 (b), the distance of both $S_{V\text{-}V}$ and $S_{H\text{-}H}$ (e.g., the adjacent unit lines distance between point N to O and O to Q) is larger enough as compared with the distance between two parallel adjacent unit lines (i.e., the distance between #1 and #3 unit lines, etc.). The $V_{near\text{-}end}$ can be neglected. Thus, the TDT waveform at the receiving end is mainly affected by $V_{far\text{-}end}$ in the proposed helix delay line.

IV. RPs TO INCREASE THE MUTUAL-CAPACITANCE OF ADJACENT UNIT LINES SECTION OF HELIX DELAY LINE

RPs are regularly added and aligned at the center of the two parallel adjacent unit lines of the helix delay line. As mentioned in Section II, the amplitude of FEXT is determined by the difference between the inductive coupling ratio (L_m/L_s) and the capacitive coupling ratio (C_m/C_T). Therefore, the design topology of FEXT

reduction in the proposed helix delay line with microstrip geometry is to increase the C_m. In order to minimize the difference between inductive coupling ratios and capacitive coupling ratios, in term of adding RPs at the center of the two parallel adjacent unit lines of the helix delay line, the FEXT formula is represented by (2).

In order to develop the design rule of RPs, and the spacing between adjacent RPs in the helix delay line, firstly, the helix delay line with RPs should be divided into several parallel three-coupled lines sections (the cross-sectional view of helix delay line with RPs structures) and several two-coupled lines sections (the cross-section view of the helix delay line without RPs structures), as shown in Fig. 3. Secondly, two equations are presented to achieve the self-capacitance and the mutual-capacitance of a parallel three-coupled lines section of helix delay line, as shown in (3) and (4). Due to the assumption that the surrounding conductors are not ferromagnetic, both parallel three-coupled lines and two-coupled lines sections of helix delay line with the dielectric can be replaced by using the air. Thus, it can achieve their self-inductance and mutual-inductance values. Finally, an industry case is described in detail and presented. This part presents the increasing of mutual-capacitance in the helix delay line with adding RPs in its adjacent parallel lines section to reduce the FEXT. In this paper, the width and the length of each RPs are denoted as L_R and D_R. The distance between two edges of adjacent RPs is denoted as G, as shown in Fig. 1 (b). The RPs design starts from determining the physical dimensions of L_R and D_R. The L_R and D_R of each RPs should be shorter than the one-tenth wavelength of the system rise time. The rise time typically takes a signal to transition between its magnitude within 10 ~ 90% edge rate [19]. In addition, to neglect the mutual coupling from adjacent RPs, the distance between adjacent RPs should be no shorter than three times of the D_R of RPs. Finally, the width and the length of each RPs can be achieved as the design above.

A. Equivalent inductance and capacitance circuit models in the three-coupled lines section

In Fig. 3, we assume that the cross-sectional dimensions of parallel three-coupled lines and two-coupled lines sections of helix delay line are different in the Z direction. The per-unit-length capacitance and inductance will be the functions of position in Z direction. For an example, *C(Z)* and *L(Z)*. This non-uniform transmission line is not easy to be solved because the resulting of per-unit-length parameters will be the functions of the independent variables in the same fashion as a non-constant coefficient ordinary differential equation. In addition, by making the approximation of the gap between consecutive patches in the *Z* direction, it significantly increases the size than in the *X* direction. Thus, per-unit-length parameters will be the functions of positions *X*, these approximations can be reached by neglecting the fringing of the field [22]. Thus, the lumped circuit approximation method in this paper is used to present the circuit model of each parallel uniform three-coupled lines section and each parallel uniform two-coupled lines section. Besides, it also adds the representations of them for FEXT calculation. For example, in the two-coupled lines section, the cross section of helix delay without RPs structures, it is easy to achieve all inductance and capacitance values for evaluating the NEXT and FEXT. An example in the three-coupled lines section, the cross section of helix delay with RPs structures, equation (3) [23], and (4) are presented in this paper to achieve the equivalent values of self-capacitance and mutual-capacitance. The equivalent values of the mutual-capacitance (i.e., C'_m) and the self-capacitance (i.e., C'_{11}) on three-coupled lines section can be directly derived as:

$$C'_m = C_{31} + \frac{C_{21} \cdot C_{32}}{C_{2g} + C_{21} + C_{32}}, \tag{3}$$

$$C'_{11} = C_{11} + \frac{C_{21} \cdot C_{21}}{C_{2g} + C_{21} + C_{32}}, \tag{4}$$

where C_{11} is the self-capacitance of aggressor line, C_{22} is the self-capacitance of patch, C_{31} is the mutual-capacitance between aggressor line and victim line, C_{21} and C_{32} are the mutual-capacitance between patch and unit line, C_{2g} is the self-capacitance of the patch to ground, and $C_{2g} = C_{22} - C_{21} - C_{32}$. Based on the assumption that the cross-section of the three-coupled lines section is a symmetrical geometry, and RPs is aligned at the center of the two-unit lines, the $C_{21} = C_{32}$. From (3), increasing the C_{21} and C_{32} will get higher C'_m which can significantly lower the difference between the inductive and the capacitive coupling ratios. Because the aggressor and victim lines of the three-coupled lines section are symmetrical geometries, the $C'_{11} = C'_{33}$. The capacitance circuit model of the three-coupled lines section and its equivalent circuit model are shown in Fig. 4 and Fig. 5, respectively.

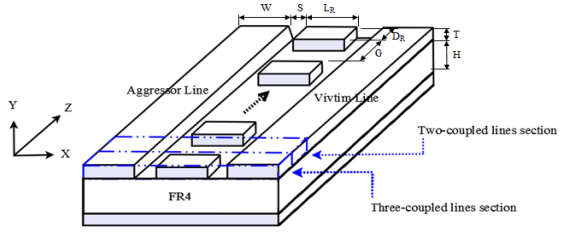

Fig. 3. A cross-sectional view of the two parallel adjacent unit lines with RPs structures.

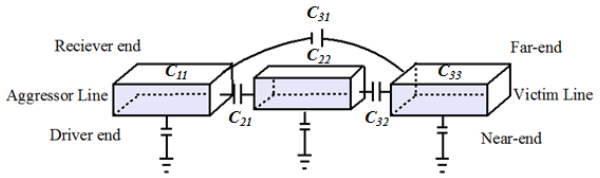

Fig. 4. A capacitance circuit model of helix delay line with RPs.

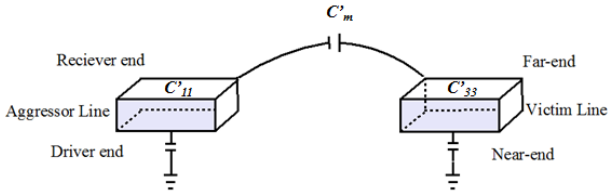

Fig. 5. An equivalent capacitance circuit model of helix delay line with RPs.

Let us assume that any medium surrounding the conductors are not ferromagnetic in the helix delay line and permeability of free space $\mu = \mu_0$. We designate the capacitance matrix with the surrounding medium removed and replaced by free space having permeability ε_0 and permeability μ_0 as C_0. Since inductance depends on the permeability of the surrounding medium and does not depend on the permittivity of the medium, the inductance matrices either self-inductance or mutual-inductance can be obtained from C_0 using the relations for a homogeneous medium, given as [24]:

$$L = \mu_0 \varepsilon_0 C_0^{-1}. \quad (5)$$

B. RPs parameters study

Figure 6 shows the simulation results of FEXT observed in two adjacent parallel lines with varying the S between the RPs and two adjacent parallel lines when dimensions are selected by W = 0.66 mm, H = 0.4 mm, T = 0.035 mm. As can be seen in Table 1, it is evident that the FEXT reduction can reach by 5.2% when the RPs dimensions are selected with L_R = 0.66 mm, D_R = 0.75 mm, and S = 0.1 mm, compared to the two parallel adjacent lines without RPs. Additionally, when the cases of S = 0.075 mm and S = 0.05 mm, the larger value of mutual-capacitance C_m can increase the ratio of C_m to C_T. The FEXT reductions can reach 13.6% and 33.7%. All results are simulated by a 3-D full-wave CST simulator [25] with a single-ended step signal of 50 ps rise time. Figure 7 compares the simulated TDT waveforms of varying L_R of RPs when considering a twenty-unit lines helix delay line with RPs structures. The dimensions are with W = 0.4 mm, H = 0.27 mm, D_R = 0.1 mm, G = 0.3 mm, T = 0.045 mm, $S_{H\text{-}H}$ = 1.2 mm, $S_{V\text{-}V}$ = 1.6 mm, ε_r = 4.3, and loss tangent = 0.035.

All simulation are implemented by a 3-D CST simulator, and the input source is chosen as a single-ended step signal with 50 ps rising time. In Fig. 7, the TDT voltage drops around 0.7-0.8ns on the case of helix delay line without RPs design because the FEXT accumulating at receiving end. A contrast to the helix delay line with RPs design, when the dimensions are selected with L_R = 0.45mm, L_R = 0.4mm, and L_R = 0.35 mm, the voltage drop has a visible reduction to the case of helix delay line without RPs design. Besides, the simulation results indicates that the smaller distance between the unit line and RPs on the case with L_R = 0.45mm (S = 0.075mm), the number of voltage drop has smallest one among four cases. It means that the smallest distance has the largest number of C_m between unit line and RPs. Figure 8 and Fig. 9 compare the simulation results for both transmission and reflection coefficients of the proposed helix delay line with RPs structures and without RPs structures. It shows that the helix delay line with RPs structures can maintain the acceptable level of transmission and reflection coefficients compared to the case of helix delay line without RPs.

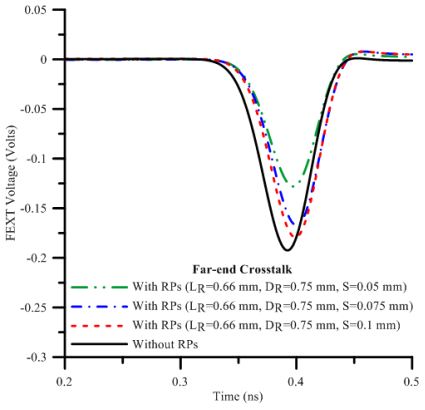

Fig. 6. The simulated waveform of FEXT.

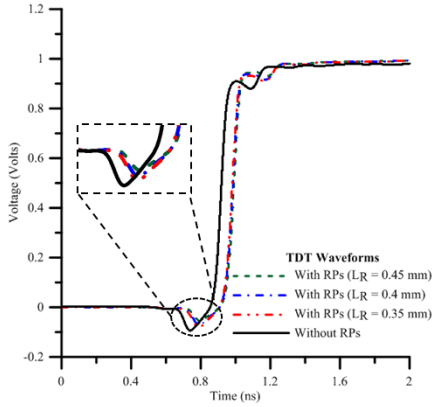

Fig. 7. The simulated TDT waveforms with varying the width of RPs.

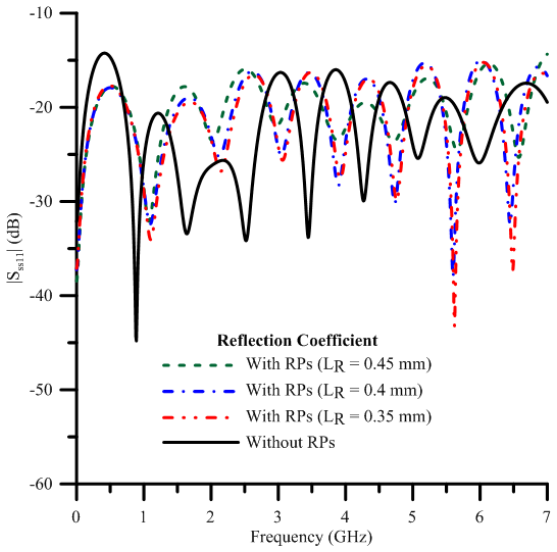

Fig. 8. The simulated reflection coefficient with varying the width of RPs.

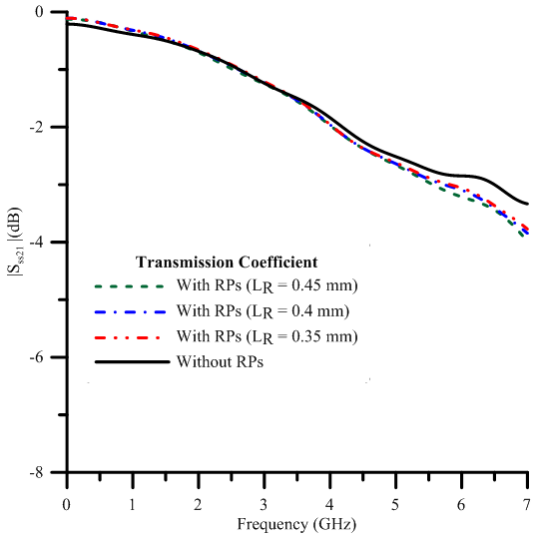

Fig. 9. Simulated transmission coefficient with varying the width of RPs.

Table 1: Simulated results of FEXT

Geometry	**FEXT (Volts)**
Two parallel adjacent unit lines without RPs	-0.193
Two parallel adjacent unit lines with RPs (L_R=0.66mm, D_R=0.75mm, S=0.1mm)	-0.183
Two parallel adjacent unit lines with RPs (L_R=0.66mm, D_R=0.75mm, S=0.075 mm)	-0.167
Two parallel adjacent unit lines with RPs (L_R=0.66mm, D_R=0.75mm, S=0.05mm)	-0.128

V. MEASUREMENT VALIDATION

The time-domain input source is selected as a single-ended step signal with an amplitude VS and the rise time t_r launched by the voltage source. Input source is connected to the driver at the end of the helix delay line in the top layer. The single-ended impedance of each unit line section of the helix delay line is 50 Ω. The source and the load resistances are chosen as R_S = R_L = 50 Ω. The load resistor is connected to the receiving end. The time-domain and the frequency-domain simulations are performed by 3-D CST full-wave simulator. Keysight 86100C TDR and E5071C VNA are used to perform measurement validations of time-domain and frequency-domain. The schematic setup is shown in Fig. 10. There are four schemes to verify the crosstalk reduction on the proposed helix delay line with RPs structures which are based on the common setting, such as the physical length between the source end to the receiving end, a number of unit lines, the spacing between adjacent unit lines, and the circuit size of the PCB.

The following four delay lines are compared. The first is the proposed helix delay line with thirteen-unit lines (1). The dimensions are with W = 0.45 mm, H = 0.305 mm, T=0.045 mm, $S_{H\text{-}H}$=2.25 mm, $S_{V\text{-}V}$=2.25 mm, FR4 with ε_r = 4.3, loss tangent = 0.035 and all spacing between adjacent unit lines are 0.6 mm. The second is the proposed helix delay line with RPs structures (2). The dimensions are with W = 0.45 mm, L_R = 0.45 mm, D_R = 0.1 mm, S = 0.075 mm and G = 0.3 mm. The third is the dimensions in serpentine delay line (3) and the fourth is the spiral delay line (4) with W = 0.45 mm, H = 0.305 mm, T=0.045 mm, FR4 with ε_r = 4.3, loss tangent = 0.035 and all spacing between adjacent unit lines are 0.6 mm, as shown in Fig. 11.

In eye-diagram between two cases of helix delay line with RPs and the case of helix delay line without RPs, it shows that the increment of the mutual-capacitance improves the waveform quality of the eye diagram. Because the RPs are added in the helix delay line, the eye-opening can be increased by 0.05 V. Figure 12 (a) and Fig. 12 (b) presents that the overshooting and undershooting can be reduced by 0.048 V and 0.049 V. As can be seen in Fig. 12 (b) and Fig. 12 (c), the overshooting and undershooting in the eye-diagram of helix delay line with RPs structures can significantly reduce by ((0.165 - 0.035) / 0.165) × 100% = 78.8% and ((0.169 - 0.043) / 0.169) × 100% = 74.6% compared to serpentine delay line. Besides, the crosstalk accumulates the receiving end of the serpentine delay line and appears as the undershooting and overshooting in the eye-diagram, as shown in Fig. 12 (c). Similarly, as can be seen in Fig. 12 (b) and Fig. 12 (d), the overshooting and undershooting in the eye-diagram of helix delay line with RPs structures can significantly reduce by ((0.069 - 0.035) / 0.069) ×

100% = 49.3% and ((0.075 - 0.043) / 0.075) × 100% = 42.7% compared to spiral delay line.

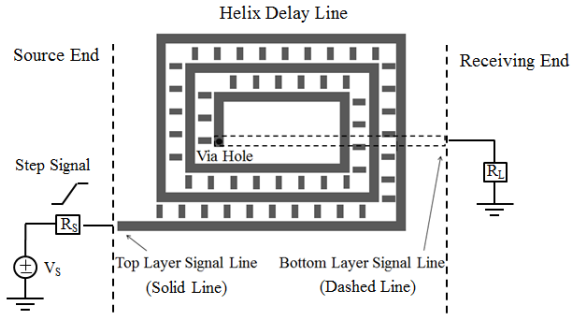

Fig. 10. The graphical schematic for time-domain simulation and measurement.

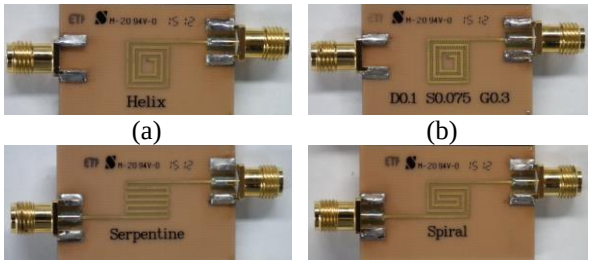

Fig. 11. The photographs of fabricated delay line. (a) The helix delay line; (b) the helix delay line with RPs structures; (c) the serpentine delay line; (d) the spiral delay line.

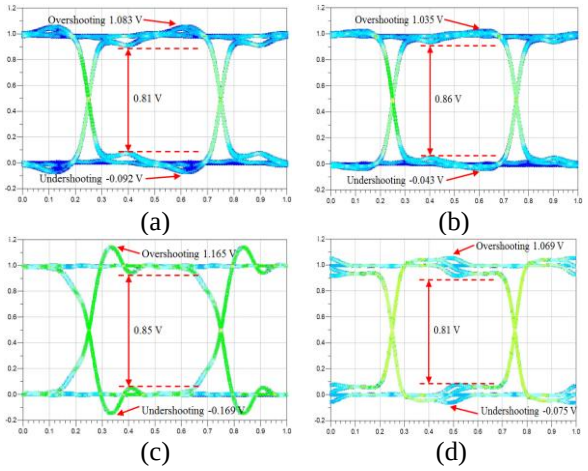

Fig. 12. The measurement results of eye-diagram. (a) The helix delay line; (b) the helix delay line with RPs; (c) the serpentine delay line; (d) the spiral delay line.

In Fig. 13, the helix delay line with RPs structures can significantly increase the mutual-capacitance and minimize the difference between the inductive with the capacitive coupling ratios. Thus, the helix delay line with RPs structures can significantly reduce the TDT waveform penalty around 0.6 ns. Keysight 86100C TDR measures the results with single-ended ramped step signal of 50 ps rise time. Figure 14 and Fig. 15 compare the measurement results of the transmission and reflection coefficients for the helix delay line without RPs, the helix delay line with RPs, the serpentine and the spiral delay lines. The results are measured by Keysight E5071C VNA. In Fig. 14 and Fig. 15, the helix delay line with RPs structures can maintain a significant level of both transmission and reflection coefficients compared to others. Thus, the proposed helix delay line with RPs does not spoil the signal transmission.

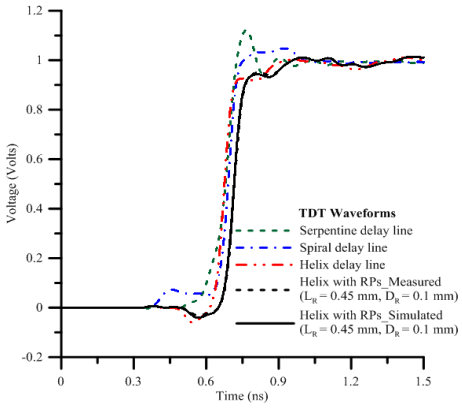

Fig. 13. The comparison between simulation and measurement of TDT waveforms.

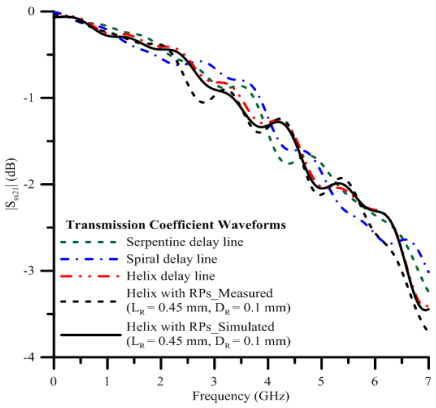

Fig. 14. The comparison between simulation and measurement of transmission coefficient.

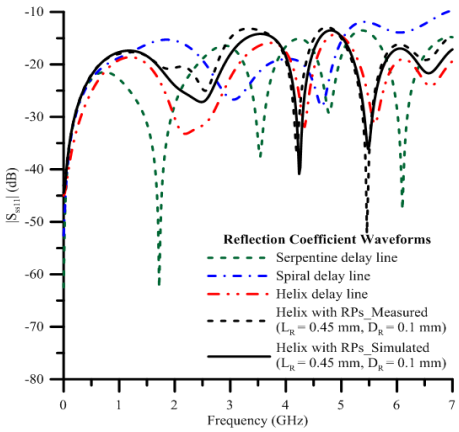

Fig. 15. The comparison between simulation and measurement of reflection coefficient.

VI. CONCLUSION

3W spacing, guard trace with ground-via, guard trace with terminators, a homogeneous dielectric substrate, grapheme coated, adding capacitors on between adjacent lines, and using RSR are common methods applied to the crosstalk reduction in past studies. Although there are with good crosstalk reduction performance, yet many ground-via, homogeneous dielectric substrate, graphene, and capacitors will increase the manufacturing cost and ground-via. Besides, the capacitors will limit the routing flexibility. In contrast to the proposed helix delay line with RPs structures, it does not need many ground-via, terminators, capacitors, and extra covering materials. Thus, it efficiently decreases the manufacturing cost, mitigates the limitation of the routing area, and reduces the routing space for reaching a miniature design. Besides, compared to the conventional packed serpentine and spiral delay lines, the NEXT is a dominant noise that is accumulated at the receiving end. The NEXT always exists and may affect the system-level timing that causes error switching in logic gates. The proposed novel helix delay lines, FEXT is a dominant noise, it can be significantly reduced with RPs. The RPs was used to significantly increase the mutual-capacitance between adjacent parallel lines of the helix delay line.

In simulation and measurement results, the helix delay line with RPs structures can significantly reduce the FEXT compared to the helix delay line without RPs structures. Besides, it improves the quality of the eye-diagram compared to the conventional serpentine and spiral delay lines. Some comparisons with the others conventional delay lines are also made to evaluate the transient TDT waveform. It is also found that the proposed helix delay line with RPs structure design has lower overshooting and undershooting voltage which can maintain eye-diagram quality.

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APPENDIX

RPs design for increasing mutual-capacitance in two parallel adjacent unit lines

In this section, in order to make a clear view about the increasing of mutual-capacitance in two parallel adjacent unit lines by adding the RPs structures, an industrial case of the two parallel adjacent lines with the length of 0.05025 m was adapted. Besides, we also provide the comparison between the proposed circuit model and 3-D full-wave simulation. The two-coupled lines section of this industrial case (i.e., the cross-sectional view of two parallel adjacent unit lines without RPs section) is shown in Fig. 3. The dimensions are with W = 0.66 mm, H = 0.4 mm, T = 0.035 mm. The spacing between adjacent unit lines is 0.86 mm. The length of each two-coupled lines section is 2.25 mm. The values of the mutual-capacitance, the self-capacitance, mutual-inductance, and self-inductance are C_m = 3.29 pF/m, C_T = 110 pF/m, L_m = 28.9 nH/m and L_S = 319 nH/m, extracted from Keysight ADS circuit simulator.

Table 2: Inductive and capacitive values of the three-coupled lines section

Capacitance (pF/m)					
C_{11}	C_{21}	C_{22}	C_{32}	C_{33}	C_{31}
128	36.3	150	36.3	128	0.91
Inductance (nH/m)					
L_{11}	L_{21}	L_{22}	L_{32}	L_{33}	L_{31}
284	*103*	*259*	*103*	*284*	*35.9*

The three-coupled lines section of this industrial case (i.e., the cross-sectional view of two parallel adjacent unit lines with RPs section) is shown in Fig. 3. The RPs are aligned regularly at the center of the two adjacent lines. The dimensions are L_R = 0.66 mm, D_R = 0.75 mm and S = 0.1 mm. The values of the mutual-capacitance, the self-capacitance, the mutual-inductance, and the self-inductance in the three-coupled lines section are listed in Table 2, extracted from Keysight ADS circuit simulator as well. The equivalent values of the mutual-capacitance and the self-capacitance in the three-coupled lines section would be achieved through (3) and (4). Their equivalent values of the self-inductance and the mutual-inductance can be achieved through (5). The equivalent values are with C_m = 9.69 pF/m, C_T = 136.8 pF/m, L_m = 29.7 nH/m and L_S = 218 nH/m. We assume that the noise source on the aggressor line was driven with the step single-ended signal, and the rise time of step signal is 50 ps. The current velocity is 1.66×10^8 m/s (i.e., 1.66×10^8

m/s = 1 / ((136.8 pF/m + 9.69 pF/m) × (218 nH/m + 29.7 nH/m))$^{1/2}$). Therefore, both dimensions of L_R and D_R of each RPs should be shorter than 0.83 mm (i.e., 0.83 mm = ((1.66×10^8 m/s) × (50 ps)) / 10).

Finally, the lumped values of inductance and capacitance of each two-coupled lines section and each three-coupled lines section can be added together to calculate the FEXT. In this industrial case, the length is 0.03825 m of two-coupled lines section (i.e., 0.03825 m = 17 × 2.25 mm, 17 two-coupled lines sections) and 0.012 m of three-coupled lines section (i.e., 0.012 m = 16 × 0.75 mm, 16 three-coupled lines sections) when the total length of the parallel adjacent lines is 0.05025 m. The lumped values are with C_m = 4.82 pF/m (i.e., 4.82 pF/m = (3.29 pF/m × 0.03825 m) / 0.05025 m + (9.69 pF/m × 0.012 m) / 0.05025 m), C_T = 117 pF/m (i.e., 117 pF/m = (110 pF/m × 0.03825 m) / 0.05025 m + (136.8 pF/m × 0.012 m) / 0.05025 m), L_m = 29.1 nH/m (i.e., 29.1 nH/m = (28.9 nH/m × 0.03825 m) / 0.05025 m + (29.7 nH/m × 0.012 m) / 0.05025 m) and L_S = 295 nH/m (i.e., 295 nH/m = (319 nH/m × 0.03825) / 0.05025 m + (218 nH/m × 0.012 m) / 0.05025 m). Therefore, all capacitance and inductance coupling ratios, including two-coupled lines section (i.e., 0.0299 = (3.29 pF/m / 110 pF/m), 0.0906 = (28.9 nH/m / 319 nH/m)), equivalent three-coupled lines section (i.e., 0.0708 = (9.69 pF/m / 136.8 pF/m), 0.1362 = (29.7 nH/m / 218 nH/m)), lumped two-coupled lines section and equivalent three-coupled section (i.e., 0.0412 = (4.82 pF/m / 117 pF/m), 0.0986 = (29.1 nH/m / 295 nH/m)), are listed in Table 3.

Table 3: Inductive and capacitive coupling ratios

Coupling Ratios	Two-Coupled Lines Section	Equivalent Three-coupled Lines Section	Lumped Two-coupled Lines Section and Equivalent Three-coupled Lines Section
$\lvert C_m/C_T \rvert$	0.0299	0.0708	0.0412
$\lvert L_m/L_S \rvert$	0.0906	0.1362	0.0986
$\lvert L_m/L_S \rvert - \lvert C_m/C_T \rvert$	0.0607	0.0654	0.0574
$\lvert L_m/L_S \rvert + \lvert C_m/C_T \rvert$	0.1205	0.2070	0.1398

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