A Physics-based Transient Simulation and Modeling Method for Wide-frequency Electrical Overstress Including ESD

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Abstract ─ Circuits design that meets various IEC electrical overstress (EOS) standards is still a challenge, for that different kinds of EOS are at different frequency bands. In this paper, a physics-based transient simulation and modeling method is proposed, which can simulate wide-frequency EOS including electrostatic discharge (ESD) and AC characteristics. In this method, the physical model is used to characterize the nonlinear semiconductor devices in the finite-difference time-domain (FDTD)-SPICE co-simulation. Moreover, the modeling and physical parameters extraction method of the ESD protect devices, the transient voltage suppressor diode, is demonstrated. Taking an EOS protection circuit for example, it is modeled and simulated by the proposed method. Moreover, the circuit is also simulated by the widely-used System-Efficient ESD Design (SEED) method, in which the TVS diode is modeled based on 100 ns Transmission Line Pulse (TLP) measurements. The experiments show that both this method and SEED method can characterize the IEC system-level ESD behaviors well. However, the error of the SEED is about 219.2% at 10 MHz AC characteristics, but the maximum error of the proposed method is only 7.8%. Hence, compared with the widely-used SEED method, this method is more accurate when characterizing the EOS event during AC operation and switching.

Index Terms ─ Electric overstress, electrostatic discharge (ESD), transient simulation, wide-frequency.

I. INTRODUCTION

An electrical device suffers an EOS event when a maximum limit for either the voltage across, the current through, or power dissipated in the device is exceeded [1]. EOS causes immediate damage or malfunction, or latent damage resulting in an unpredictable reduction of its lifetime. The worldwide survey results show greater than 20% of total failures being EOS-related or 30% of total electrical failures being EOS-related [2]. The accurate simulation of EOS events enables the design of reliable protection on the first attempt and avoids the need for repeated design optimization tests [3]. The root causes leading to EOS include ESD [4], switching or alternating current (AC) applications [5, 6], and so on.

Among the simulation of EOS events, system-level ESD simulation is widely-concerned and well-studied. The SEED methodology is widely used for system-level ESD design. The SEED emphasizes the analysis of the interaction between the quasi-static I–V curve of a vulnerable protection element. Li *et al.* model and simulates transient response of a keypad backlight LED circuit in a smartphone under IEC 61000-4-2 excitation [7]. Scholz *et al.* present a TLP and HMM tests-based methodology which combines on-wafer characterization and transient simulation for the system-level ESD protection design [8, 9]. Wei *et al.* adopt SEED method to analyze interactions between external ESD protection device and the on-chip ESD protection circuit in a high-speed USB3.x IO circuit [10]. However, these studies only concern the ESD responses. That is to say, the accuracy for simulating other kinds of EOS root cause events is not validated, such as AC characteristics. Because a circuit or product must meet all kinds of EOS qualifications, and the accurate simulation of AC characteristics is essential for characterizing the EOS event during AC operation and switching.

Moreover, an accurate model of transient voltage suppressor (TVS) devices is critical to decide if the protection solutions are overdesigned or failed in the EOS tests. In the existing studies, the ESD protection components models are built by various methods. Zhang *et al.* use Hardware Description Language to describe the TLP-based behavioural model [11, 12]. Li *et al.* model the ESD protection devices by consisting of several compact model elements to accurately simulate the device behaviours under ESD stress conditions [13]. Pan *et al.* develop a physics-based model to model the conductivity modulation under an ESD stress [14]. Meng *et al.* present a piecewise-linear model with transient relaxation to describe the nonlinear transient characteristics of ESD protection devices [15]. But the models in these existing studies have only been validated by simulating responses to system-level IEC 61000-4-2 pulses, and the responses during AC operation are not

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simulated and validated.

In this paper, we adopt physics-based field-circuit co-simulation to realize the EOS simulation. In this method, the physical model is used to characterize the nonlinear semiconductor devices, because physical models show great advantages in analyzing the circuits over wide frequencies [16, 17] and wide power ranges [18, 19]. The physics-based circuit simulation solves the carrier transport equations to model the semiconductor devices, and then the semiconductor devices' numerical physical model is incorporated into an equivalent-model based circuit simulation to analyze the whole circuits. Then the lumped circuit simulation is hybridized with the FDTD simulation by interfacing EM (electromagnetic) field quantities with lumped-element quantities at each timestep. The main feature that distinguishes this method from the field-circuit coupling methods [20, 21] is the physical modeling method of semiconductor devices. The main feature that distinguishes this method from the physical model-based methods [22, 23] is that this method involves electromagnetic computation. Moreover, the modeling and physical parameters extraction method of the ESD protect devices, the transient voltage suppressor diode, is demonstrated. Finally, taking an ESD protection circuit for example, it is modeled and simulated by the proposed method and also the widely-used SEED method.

II. SYSTEM-LEVEL EOS SIMULATION METHOD

In the physics-based system-level EOS simulation method, the simulation model is divided into two parts, the full-wave part, and the nonlinear-circuit part. In each timestep, the EM simulation and circuit simulation are coupled by an FDTD-SPICE linking method.

In the linear full-wave part, such as distributed electromagnetic structure such as the PCB circuit and the air around the circuit, the FDTD method [24] is used to solve Maxwell's equations, as (1-2):

$$\nabla \times \mathbf{E} = -\mu \frac{\partial \mathbf{H}}{\partial \mathrm{t}}, \tag{1}$$

$$\nabla \times \mathbf{H} = \mathbf{J} + \varepsilon \frac{\partial \mathbf{E}}{\partial \mathrm{t}}. \tag{2}$$

In the nonlinear circuit solving part, the physical model-based lumped circuit simulation is used to solve the circuit responses. Specifically, the Newton-Raphson method is used to solve Kirchhoff's current equation, as in (3). According to Kirchhoff's current equation, the sum of all currents leaving a node is zero. Assume that a circuit element is located between *(k-1)*th and *k*th node, the relationship between its current I_j and node voltage U_k and U_{k-1} is described in (4):

$$\sum I_j = 0, \tag{3}$$

$$I_j = \psi(U_k, U_{k-1}). \tag{4}$$

Hence, each element in the nonlinear circuit is characterized by the voltage-current relationship. For a relatively simple circuit element, such as a resistor or a capacitance, the relationship in (4) can be obtained by the analytic equation. For a critical semiconductor device, to obtain its voltage-current relationship in (4), it is modeled by the drift-diffusion physical model, as the equation group (5-9) [25]. The semiconductor device physical model is adopted to characterize the nonlinear semiconductor devices, and used to characterize the behaviours of the electric field, electron concentration, and hole concentration inside the nonlinear semiconductor devices. The physical model is selected because it is more applicable for simulating devices in high voltage and large current operations [19]. The voltage-current relationship of the semiconductor device can be obtained by solving the discrete equations of (5-9) in time domain by the finite difference method:

$$\mathbf{J}_{\mathrm{n}} = qD_{\mathrm{n}}\nabla n - q\mu_{\mathrm{n}} n\nabla\varphi, \tag{5}$$

$$\mathbf{J}_{\mathrm{p}} = -qD_{\mathrm{p}}\nabla p - q\mu_{\mathrm{p}} p\nabla\varphi, \tag{6}$$

$$\partial n/\partial t = q^{-1}\nabla\cdot\mathbf{J}_{\mathrm{n}} + G - R, \tag{7}$$

$$\partial p/\partial t = -q^{-1}\nabla\cdot\mathbf{J}_{\mathrm{p}} + G - R, \tag{8}$$

$$\nabla\cdot(\varepsilon_s\nabla\varphi) = q(n - p + N_A - N_D). \tag{9}$$

Equation (5) and (6) are current equations for electrons and holes in a semiconductor, equation (7) and (8) are continuity equations for electron and hole, equation (9) is Poisson's equation. J_n and J_p are the electron and hole current densities, q is the electronic charge, D_n and D_p are the hole and electron diffusion coefficients, n and p are the electron and hole density respectively, μ_n and μ_p are the hole and electron mobility respectively, φ is the electric potential, t is time, ε_s is the permittivity of the semiconductor material, R is electron-hole recombination rate, G is electron-hole generation rate, N_A is acceptor impurity concentration, and N_D is donor impurity concentration.

For the simulation of the TVS diode in this work, the ohmic contacts are implemented as boundary conditions. Hence, the electron concentration, hole concentration, and potential on the surface can be expressed as equations (10-12),

$$n_{\mathrm{s}} = 0.5\cdot[N_D - N_A + \sqrt{(N_D - N_A)^2 + 4n_{ie}^2}, \tag{10}$$

$$p_{\mathrm{s}} = \frac{n_{ie}^2}{n_{\mathrm{s}}}, \tag{11}$$

$$\varphi_{\mathrm{s}} = V_{\mathrm{s}} - \ln p_{\mathrm{s}}, \tag{12}$$

where n_{s}, p_{s}, φ_{s}, n_{ie} are the electron concentration, hole concentration, potential, and Intrinsic carrier concentration on the surface, respectively.

The initial values of the electron concentration, hole concentration, and potential affect the solving time and whether convergence can be achieved. Here, the dc initial value at N type doping zone is as:

$$n = N(x), \tag{13}$$

$$p = \frac{1}{N(x)}, \tag{14}$$

$$\varphi = \ln N(x). \tag{15}$$

The initial value at P type doping zone is as:

$$n = -\frac{1}{N(x)}, \tag{16}$$

$$p = -N(x), \tag{17}$$

$$\varphi = -\ln[-N(x)]. \tag{18}$$

After calculating the dc solution, the dc solution is used in the AC analysis as initial values.

By using the boundary condition (10-12) and initial value (13-15), the equations (5-9) are solved, so that the voltage-current relationship of the semiconductor device can be obtained.

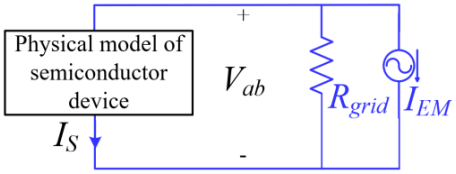


Fig. 1. The parallel circuit formed in FDTD-SPCIE linking procedure.

The FDTD-SPICE linking method [26] is used to couple the EM simulation and nonlinear circuit simulation. By discretization and transforming, equation (2) can be transformed into:

$$V_{ab}^{n+1} = [(I_x^{n+1})_{EM} - I_{sx}^{n+1}](R_x^{n+1})_{grid}, \tag{19}$$

where I_{EM}, R_{grid}, and I_S can equivalently form a parallel lumped circuit, as shown in Fig. 1. R_{grid} and I_{EM} are the equivalent circuit model of the distributed electromagnetic structure; I_S is the current through the semiconductor device. In the FDTD-SPICE linking procedure, I_{EM} and R_{grid} are calculated and used to characterize the effect of the "field" to "circuit" firstly. Then they are passed to the nonlinear circuit solving part, and the formed parallel circuit is calculated by the physical model-based lumped circuit simulation. Hence, the current through the semiconductor device I_S can be obtained. I_S characterizes the influence of the "circuit" to "field. Then the electric field is updated using I_S at the location where the semiconductor device is located. In this way, the physical-model circuit simulation and FDTD field simulation are integrated into a unified scheme. The specifics of this method can be found in previous work [27].

III. TVS DIODE PHYSICAL MODEL

The TVS diode is modeled by the diode chip's physical model and the package's equivalent circuit model, as shown in Fig. 2.

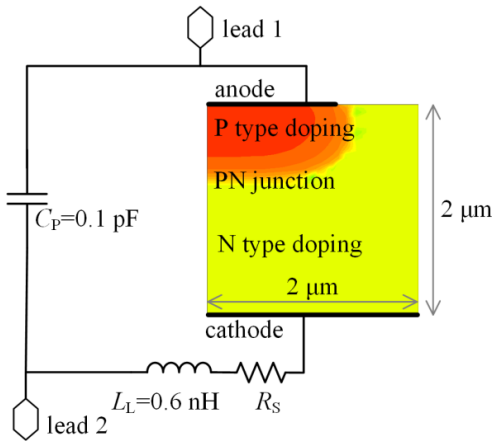


Fig. 2. TVS diode chip's physical model and package's equivalent circuit model.

In the package's equivalent circuit model, C_P represents the package capacitance, and L_L represents the lead inductance. To obtain the values of the two package circuit elements, the small-signal scattering parameters of two TVS diode circuits are measured. The TVS diode microstrip circuits are shown in Fig. 3. In the circuit of Fig. 3 (a), the TVS diode is connected between the centre of the microstrip line and a grounding via. In the circuit of Fig. 3 (b), the TVS diode is connected among the gap of the microstrip line. For the two circuits, the left and right end of the microstrip is port 1 and port 2, respectively. To measure the scattering parameters, the two ports are connected to vector network analyser Agilent N5230A through SMA connectors. Using the genetic algorithm, the value of C_P and L_L are adjusted, so that the simulated scattering parameters can fit the measured ones well.

To compute the scatting parameters of the limiter, a unit amplitude modulated Gaussian pulse is injected to the input port 1 as excitation, the reflection waveform at input port 1, and transmitter voltage waveform at output port 2 are calculated to obtain $|S_{11}|$ and $|S_{21}|$ respectively. The extracted value of C_P is 0.1 pF, and the extracted value of L_L is 0.6 nH. The measured and simulated $|S_{11}|$ and $|S_{21}|$ of the two circuits are shown in Fig. 4 (a) and 4 (b), respectively. The discrepancy at lower frequencies in $|S_{21}|$ of Fig. 4 (b) is due to the imperfect extracted component values.

(a) (b)

Fig. 3. Microstrip circuit: (a) with a series TVS diode, and (b) with a parallel TVS diode.

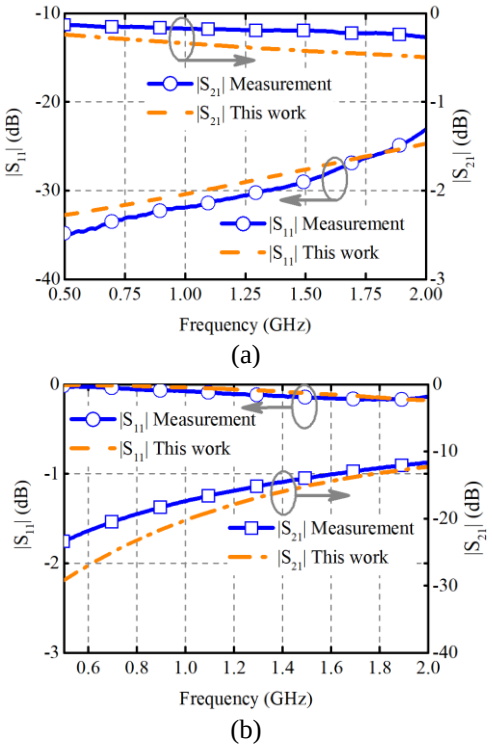


Fig. 4. Scattering parameters of TVS diode microstrip circuit: (a) series connection, and (b) parallel connection.

As shown in Fig. 2, the TVS diode chip is a P-N semiconductor junction, which is a linearly-graded junction. Hence, the unknown physical parameters that need to be extracted include P type doping concentration N_A, N type doping concentration N_D, P-N junction area A, and the substrate resistance R_S.

The physical parameters of the diode are extracted from the measurement results. The breakdown voltage of TVS diode V_{BR} is 6.8V, which is decided by the P type and N type doping concentration. Hence, the doping concentration is extracted from the value of V_{BR} based on the genetic algorithm. N_A is 8.0e15 /cm^3, and N_D is 1.2e18 /cm^3. Moreover, based on the measured DC I-V curve, the junction area A and the substrate resistance R_S are extracted, which are 0.3 mm^2 and 0.25 Ω, respectively. The simulation is based on a 2-D rectangle model, and its width is 2 μm. Hence, we need to multiply the calculated current value from the 2-D model by 1.5e5 times, so that the real diode current can be obtained.

By using the model and extracted physical parameters of the diode chip, the DC I-V curve is simulated, which agrees well with the measured curve, as shown in Fig. 5. The DC I-V curve is simulated by solving semiconductor equations (5-9).

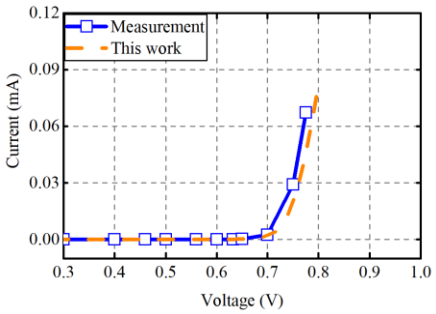


Fig. 5. Simulated and measured forward DC I-V curves.

IV. THE SEED SIMULATION METHOD

In white paper 3, the Industry Council on ESD target levels proposed the SEED methodology [2], which is used for the design of off-chip ESD protection solutions meeting system-level ESD specifications. When an IEC61000-4-2 discharge is applied to an external pin on the system board, the main ESD current flows directly to the ground through the on-board TVS, but some current will enter a connected IC. To prevent damage to the IC, it is important to assess the amount of current which may enter the IC and the associated voltage across the connected IC circuitry. Hence, it is clear that the design of on-chip ESD protection and on-board system level protection cannot be performed separately. By using the SEED method, the TLP curves of the on-chip and off-chip ESD protection devices are captured and compared. Then estimate the current and voltage operating point of the external pin for an ESD discharge event, and judge if it is outside the SOA. Hence, we can know if additional off-chip devices are required to obtain the desired system-level protection level.

To model and simulate the ESD protection circuit by SEED method, the TVS diode is modeled by both the TLP test results and the datasheet. Using the modeling method in [7], the model has two parts, as shown in Fig. 6. The factory-provided SPICE model is for nominal current conditions. The two voltage-controlled resistances are to mimic the high-current TLP I-V behaviour. Diode 2 was used as a unidirectional switch to separate the positive and negative pulse injections. Diode 1 defines the TLP I-V characteristics of the TVS diode under negative pulses applied to its cathode. Diode 3 and the switch determined the positive TLP I-V characteristics. The measured and simulated 100 ns TLP I-V curves by this model are shown in Fig. 7. The simulated curve agrees well with the measured TLP curve.

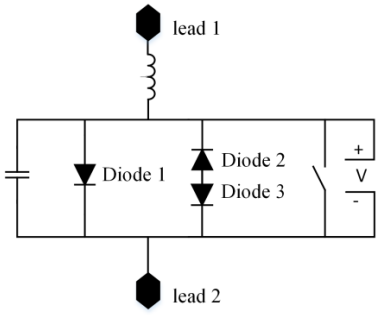


Fig. 6. TVS diode SPICE model.

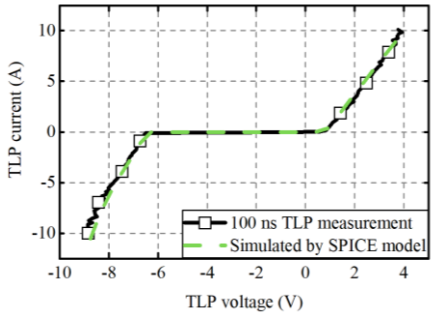


Fig. 7. TVS diode SPICE model simulation TLP results.

V. SIMULATION AND MEASUREMENT RESULTS

To validate the simulation method, a typical EOS protection circuit is simulated and measured, as shown in Fig. 8. In the circuit, a 50 Ω microstrip line is the EOS transmission path. The left end of the line is the EOS discharge point. The right end is connected to a load resistance and an SMA connector, which is connected to an oscilloscope to observe the voltage waveform. Moreover, a commercial TVS diode is a protection component and connected between the microstrip centre and a grounded via. The modeling method of each circuit element is as follows. Moreover, the ESD generator is modeled by its equivalent circuit model [7], as shown in Fig. 9. This model is selected because it can characterize the effect of load impedance and simulate efficiently.

Various responses of this circuit are simulated by the proposed method and the SEED method, including DC I-V curves, system-level ESD discharge responses, and AC characteristics. The simulated results are compared with the measured results.

The reverse DC I-V curves simulated by solving semiconductor equations (5-9) in this work, SEED method, and the measured ones are shown in Fig. 10. The simulated curve by this work shows that the breakdown voltage is 6.8V, which is consistent with the measured results. There is error between the simulated steepness of the I-V curve after the breakdown by this work and the measurement ones, because that the semiconductor equations (5-9) don't include the heat equation, so that the heat generation and its influence on the current have not been simulated. The breakdown voltage simulated by the SEED method is 6.5 V, which is slightly different with the measured results. The error from the SEED is due to the TLP measurement error.

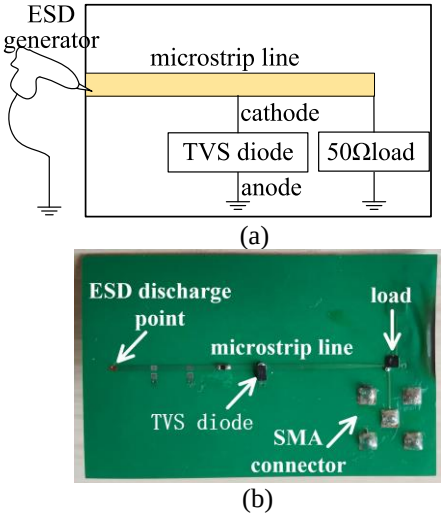


Fig. 8. EOS protection circuit: (a) circuit diagram and (b) circuit prototype.

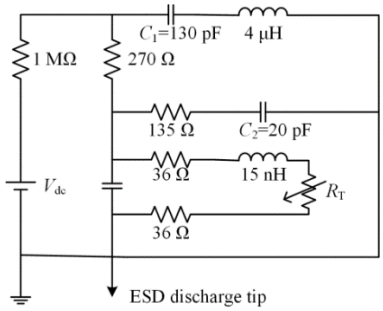


Fig. 9. ESD generator equivalent circuit.

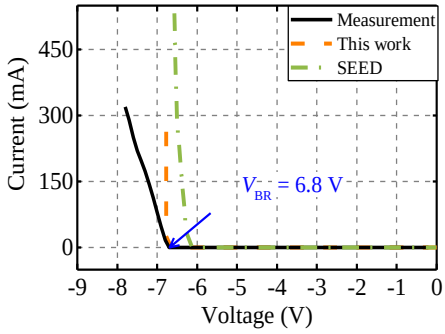


Fig. 10. Reverse DC I-V curves of the TVS diode.

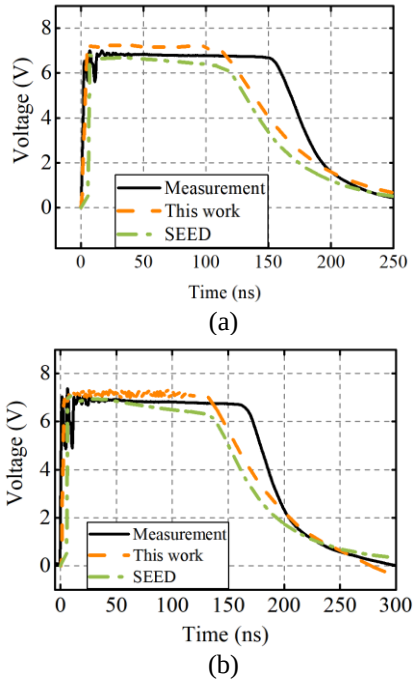
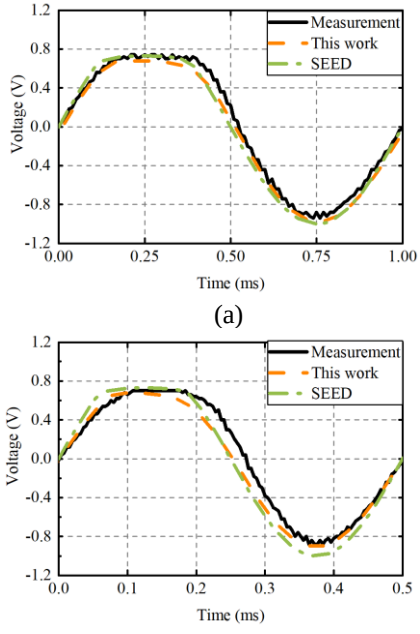
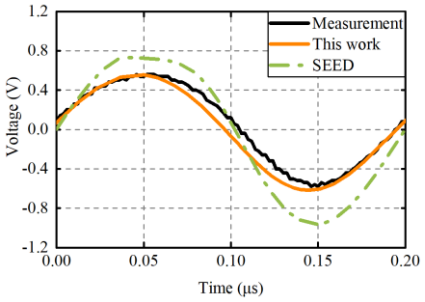


Fig. 11. Voltage waveforms of load when ESD pulse discharges. (a) 0.5 kV ESD pulse discharges. (b) 1 kV ESD pulse discharges.

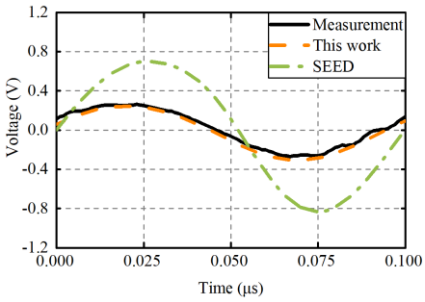
As shown in Fig. 11, the system-level IEC61000-4-2 ESD discharge responses are also simulated and measured. In each simulation timestep, the voltage value is calculated by using the equivalent circuit in Fig. 9, and is applied to the discharge point in the EOS protection circuit. Then the voltage across the TVS diode at this timestep is obtained by the proposed method. The calculation process is repeated until the last timestep. The voltage waveforms across the TVS diode are also measured. In comparison with the measurement, the simulated voltage clamping time is a little shorter, which is caused by the imperfect generator model and measurement error. But the proposed method and the SEED method both can characterize the clamping behaviours of the TVS diode well. Specifically, when the pulse amplitude is 0.5 kV, the measured voltage is 6.82 V at 50 ns. The simulated voltage by this work is 7.17 V with error of 5.0%, as shown in Fig. 11 (a). When the pulse amplitude is 1 kV, the measured voltage is 6.91 V at 50 ns, and the simulated voltage by this work is 7.23 V with error of 4.6%, as shown in Fig. 11 (b).

Figure 12 shows the simulated and measured AC voltage waveforms across the load at different frequencies. When calculating the AC characteristics, the input signal is defined as a sine wave with amplitude of 1 V at different working frequencies. As shown in Fig. 12 (a) and 12 (b), the diode shows the characteristic of rectification at low frequencies. Namely, it has low resistance in one direction and has high resistance in the opposite direction. Both the proposed method and the SEED method can characterize the voltage waveforms at 1 kHz and 2 kHz. However, as the working frequency increases, the voltage waveforms across the diode don't show the "rectification" characteristics. As shown in Fig. 12 (c) and 12 (d), the voltage waveforms become nearly sinusoidal. Meanwhile, the maximize voltages are 0.56 V and 0.29 V at 5 MHz and 10 MHz, respectively. Namely, its amplitude decreases with the frequency increases. Compared with measured results, the proposed physics-based system-level EOS simulation method agrees well with the measurement results, and can characterize these AC nonlinear behaviours well. The maximum relative error values of the simulated curves by the proposed method in Fig. 12 (c) and 12 (d) are 0.34% and 7.8%, respectively. The proposed method can accurately characterize the TVS diode impedance characteristics at a wider frequency range, because the TVS diode is modeled by its physical model, which solves the semiconductor equations. However, the maximum relative error values of the simulated curves by the SEED method are 65.5% and 219.2%, respectively. The SEED method is inaccurate at 5 MHz and 10 MHz, because the TVS diode is modeled by its TLP tests, which is equivalent to a nonlinear resistance and cannot characterize the reactance characteristics of the TVS diode. It indicates that the SEED method cannot characterize nonlinear AC characteristics, which can lead to totally wrong voltage calculations when characterizing the EOS events during AC operation and switching.





(c)



(d)

Fig. 12. AC voltage waveforms of the load at different frequencies: (a) 1 kHz, (b) 2 kHz, (c) 5 MHz, and (d) 10 MHz.

VI. CONCLUSION

This paper adopts a physics-based transient simulation and modeling method to simulate wide-frequency electric overstress. The method is the semiconductor device's physical model-based FDTD-SPICE co-simulation. Moreover, the modeling method of the TVS diodes is introduced. The experiments show that the proposed method can characterize the EOS protection circuit accurately, including DC, AC, and system-level ESD responses. Compared with the widely-used SEED method, this method can characterize nonlinear AC characteristics more accurately. This method shows advantages in designing a product that can immune from EOS.

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