

Novel Parallelization of Discontinuous Galerkin Method for Transient Electromagnetics Simulation Based on Sunway Supercomputers

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Abstract – A novel parallelization of discontinuous Galerkin time-domain (DGTD) method hybrid with the local time step (LTS) method on Sunway supercomputers for electromagnetic simulation is proposed. The proposed method includes a minimum number of roundtrip (MNR) strategy for processor-level parallelism and a double buffer strategy based on the remote memory access (RMA) of the Sunway processor. The MNR strategy optimizes the communication topology between nodes by recursively establishing the minimum spanning tree and the double buffer strategy is designed to make communication overlapped computation when RMA transmission. Combining the two methods, the proposed method achieves an unprecedented massively parallelism of the DGTD method. Several examples of radiation and scattering are used as cases to study the accuracy and validity of the proposed method. The numerical results show that the proposed method can effectively support 16,000 nodes (1,040,000 cores) parallelism on the Sunway supercomputer, which enables the DGTD method to solve the transient electromagnetic field in a very short time.

Index Terms – discontinuous Galerkin method, electromagnetic analysis, memory access optimization, sunway TaihuLight.

I. INTRODUCTION

As one of the most accurate time-domain electromagnetic field calculation methods, the discontinuous Galerkin time-domain (DGTD) method has higher numerical accuracy and modeling flexibility than traditional time-domain methods, such as the finite difference time-domain (FDTD) method and the finite volume time-domain (FVTD) method [1–3]. Thus, it is widely used in the simulation of broadband characteristics in ultra-wideband (UWB) communication, pulse radar, time-domain measurement, and electromagnetic compatibility, etc [4, 5]. In the industrial application of the DGTD method [1–3, 8, 9], the important key technologies are multi-scale techniques and the massively

parallelism techniques [10–12]. The common multi-scale technique of the DGTD method is local time stepping (LTS). At present, some research on the thread-level parallelism of LTS-DGTD [13, 20, 21], which makes the implementation of the distributed parallelism of LTS-DGTD is feasible, has been performed. However, LTS-DGTD does not scale well on the multi-node parallelism between nodes [13, 14]. The multi-node parallelism is very common in distributed platforms, such as supercomputers. With the advancement of computer technology, supercomputers have reached tens of thousands of nodes so far [13, 15–17], and the maximum parallel size of the DGTD method has stopped at hundreds of nodes [14, 18–20], which makes the DGTD method unsuitable for electrically large problems on modern supercomputers with ever increasing nodes. Therefore, the massively node-level parallelism for the LTS-DGTD method urgent. In addition, at the current situation of chip supply shortage and prohibition, it is necessary to study the parallelism of China's domestic processors, such as SW26010, which composes the Sunway TaihuLight, the most powerful supercomputer in China [21–26]. Based on SW26010, a new Sunway CPU has been developed [27]. The new Sunway CPU expands the computing processing element (CPE)'s local data memory (LDM) from 64KB to 256 KB and improves the bandwidth of the LDM controller. At the same time, the remote memory access (RMA) technology, which is one of the most attractive technological advances of the new Sunway CPU is introduced for the communication between CPEs. The new Sunway supercomputer composed of the new Sunway CPU, will be possible achieves 1000 PFlops [28]. However, there is no research on the DGTD method with the new Sunway CPU.

To solve these problems, this paper proposes a novel parallelism of the LTS-DGTD method for Sunway supercomputers. The proposed method has a minimum roundtrip strategy to improve the scalability of node-level parallelism of the LTS-DGTD method, and a double-buffer parallelism with RMA of LTS-DGTD method for the new Sunway supercomputer. The

double-buffer strategy is efficient for reducing the computing time in-cores and improves the communication efficiency of the LTS-DGTD in CPEs. These two proposed strategies enable the LTS-DGTD method to be implemented on the new Sunway supercomputer successfully and efficiently.

II. THE FORMULATION OF DISCONTINUOUS GALERKIN TIME-DOMAIN

The Maxwell's equation in 3D space [4] is:

$$\begin{cases} \nabla \times \mathbf{H} = \varepsilon \frac{\partial \mathbf{E}}{\partial t} + \mathbf{J} \\ \nabla \times \mathbf{E} = -\mu \frac{\partial \mathbf{H}}{\partial t} \\ \nabla \cdot \mathbf{D} = \rho \\ \nabla \cdot \mathbf{B} = 0, \end{cases} \quad (1)$$

in which \mathbf{E} , \mathbf{H} , \mathbf{D} and \mathbf{B} are the electric field intensity, magnetic field intensity, electric flux density, and magnetic flux density, respectively; ε is permittivity and μ is permeability, and \mathbf{J} is the electric current density; ρ is the electric charge density. \mathbf{E} and \mathbf{H} are approximated as:

$$\begin{aligned} \mathbf{E} &= \sum_i^{n_p} E_i(t) \mathbf{N}_i \\ \mathbf{H} &= \sum_i^{n_p} H_i(t) \mathbf{N}_i, \end{aligned} \quad (2)$$

where \mathbf{N}_i denotes the basis function, $E_i(t)$ and $H_i(t)$ are the time dependent coefficients of basis function \mathbf{N}_i , n_p is the number of basis functions. In this study, the 0.5, 1 and 2 order hierarchical basis functions of [6] are used.

Following the Galerkin finite elements approach [1] to the curl operators of equation (1) without \mathbf{J} , it can be written as:

$$\begin{cases} \int_{\Omega} \nabla \times \mathbf{H} \cdot \mathbf{N}_i d\mathbf{v} = \int_{\Omega} \varepsilon \frac{\partial \mathbf{E}}{\partial t} \cdot \mathbf{N}_i d\mathbf{v} \\ \int_{\Omega} \nabla \times \mathbf{E} \cdot \mathbf{N}_i d\mathbf{v} = - \int_{\Omega} \mu \frac{\partial \mathbf{H}}{\partial t} \cdot \mathbf{N}_i d\mathbf{v}, \end{cases} \quad (3)$$

where Ω is the calculation domain divided into tetrahedrons. According to [1], with integration by parts, the weak forms of equation (3) are:

$$\begin{cases} \int_{\Omega} \varepsilon \frac{\partial \mathbf{E}}{\partial t} \cdot \mathbf{N}_i d\mathbf{v} - \int_{\Omega} \nabla \times \mathbf{N}_i \cdot \mathbf{H} d\mathbf{v} \\ \quad \int_{\Gamma} (\hat{\mathbf{n}} \times \mathbf{H}) \cdot \mathbf{N}_i ds \\ \int_{\Omega} \mu \frac{\partial \mathbf{H}}{\partial t} \cdot \mathbf{N}_i d\mathbf{v} + \int_{\Omega} \nabla \times \mathbf{N}_i \cdot \mathbf{E} d\mathbf{v} \\ \quad - \int_{\Gamma} (\hat{\mathbf{n}} \times \mathbf{E}) \cdot \mathbf{N}_i ds, \end{cases} \quad (4)$$

where Γ is the boundary of Ω , and $\hat{\mathbf{n}}$ is the normal vector located on Γ . The DGTD method introduces numerical fluxes to substitute for the right-terms, i.e., integration

over the tetrahedron interfaces. We fthe procedure set out in [7] to deal with the right-terms of equation (4): solving the Riemann problem under the Rankine-Hugoniot condition yields an expression for the upwind flux:

$$\begin{aligned} \hat{\mathbf{n}} \times \mathbf{H}_i &= \hat{\mathbf{n}} \times \frac{Z_i \mathbf{H}_i + Z_j \mathbf{H}_j}{Z_i + Z_j} + \hat{\mathbf{n}} \times \hat{\mathbf{n}} \times \frac{\mathbf{E}_i - \mathbf{E}_j}{Z_i + Z_j} \\ \hat{\mathbf{n}} \times \mathbf{E}_i &= \hat{\mathbf{n}} \times \frac{Y_i \mathbf{E}_i + Y_j \mathbf{E}_j}{Y_i + Y_j} - \hat{\mathbf{n}} \times \hat{\mathbf{n}} \times \frac{\mathbf{E}_i - \mathbf{E}_j}{Y_i + Y_j}, \end{aligned} \quad (5)$$

where j is the adjacent tetrahedron of tetrahedron i , the wave impedances of i and j are $Z_i = \frac{1}{Y_i} = \sqrt{\frac{\mu_i}{\varepsilon_i}}$ and $Z_j = \frac{1}{Y_j} = \sqrt{\frac{\mu_j}{\varepsilon_j}}$, respectively. For anisotropic Maxwell equations, it is necessary to deal with the tensor matrices of permittivity and permeability, which has been well solved in [4] and [5]. The isotropy semi-discrete form with upwind flux is shown as:

$$\begin{aligned} &\int_{\Omega} \varepsilon \frac{\partial \mathbf{E}_i}{\partial t} \cdot \mathbf{N}_i d\mathbf{v} - \int_{\Omega} \nabla \times \mathbf{H}_i \cdot \mathbf{N}_i d\mathbf{v} = \\ &\int_{\Gamma} \left(\hat{\mathbf{n}} \times \frac{Z_j (\mathbf{H}_j - \mathbf{H}_i)}{Z_i + Z_j} - \hat{\mathbf{n}} \times \hat{\mathbf{n}} \times \frac{\mathbf{E}_i - \mathbf{E}_j}{Z_i + Z_j} \right) \cdot \mathbf{N}_i ds \\ &\int_{\Omega} \mu \frac{\partial \mathbf{H}_i}{\partial t} \cdot \mathbf{N}_i d\mathbf{v} + \int_{\Omega} \nabla \times \mathbf{E}_i \cdot \mathbf{N}_i d\mathbf{v} = \\ &- \int_{\Gamma} \left(\hat{\mathbf{n}} \times \frac{Y_j (\mathbf{E}_j - \mathbf{E}_i)}{Y_i + Y_j} + \hat{\mathbf{n}} \times \hat{\mathbf{n}} \times \frac{\mathbf{H}_i - \mathbf{H}_j}{Y_i + Y_j} \right) \cdot \mathbf{N}_i ds, \end{aligned} \quad (6)$$

which can be written as matrix forms as:

$$\begin{aligned} \varepsilon \mathbf{M} \frac{\partial \tilde{\mathbf{E}}_i}{\partial t} &= \mathbf{S} \tilde{\mathbf{H}}_i + \\ &\sum_{f=1}^4 \left(k_h \mathbf{F}_{\Gamma_f} (\tilde{\mathbf{H}}_j - \tilde{\mathbf{H}}_i) - v_e \mathbf{G}_{\Gamma_f} (\tilde{\mathbf{E}}_j - \tilde{\mathbf{E}}_i) \right) \\ \mu \mathbf{M} \frac{\partial \tilde{\mathbf{H}}_i}{\partial t} &= -\mathbf{S} \tilde{\mathbf{E}}_i - \\ &\sum_{f=1}^4 \left(k_e \mathbf{F}_{\Gamma_f} (\tilde{\mathbf{E}}_j - \tilde{\mathbf{E}}_i) + v_h \mathbf{G}_{\Gamma_f} (\tilde{\mathbf{H}}_j - \tilde{\mathbf{H}}_i) \right), \end{aligned} \quad (7)$$

where $\tilde{\mathbf{E}}$ and $\tilde{\mathbf{H}}$ denote vectors composed by E_i and H_i in the integral domain, respectively, the flux coefficients are $k_h = \frac{Z_j}{Z_i + Z_j}$, $k_e = \frac{Y_j}{Y_i + Y_j}$, $v_e = \frac{1}{Z_i + Z_j}$ and $v_h = \frac{1}{Y_i + Y_j}$, \mathbf{M} is the mass matrix, \mathbf{S} is the stiffness matrix, \mathbf{F} and \mathbf{G} are the flux matrices. Those matrices can be summarized:

$$\begin{aligned}
\mathbf{M} &= \int_{\Omega} \mathbf{N}_i \cdot \mathbf{N}_i dv \\
\mathbf{S} &= \int_{\Omega} \nabla \times \mathbf{N}_i \cdot \mathbf{N}_i dv \\
\mathbf{F} &= \int_{\Gamma} \hat{\mathbf{n}} \times \mathbf{N}_k \cdot \mathbf{N}_i ds, (k = i||j) \\
\mathbf{G} &= \int_{\Gamma} \hat{\mathbf{n}} \times \hat{\mathbf{n}} \times \mathbf{N}_k \cdot \mathbf{N}_i ds, (k = i||j).
\end{aligned} \quad (8)$$

Those linear equations defined in one tetrahedron or a subdomain of Ω avoid composing a large sparse matrix.

Applying the explicit leapfrog (LF) scheme [10] to deal with the time derivative of equation (7), we have:

$$\begin{aligned}
\mu \mathbf{M} \frac{\tilde{\mathbf{H}}_i^{n+\frac{1}{2}} - \tilde{\mathbf{H}}_i^{n-\frac{1}{2}}}{\Delta t} &= -\mathbf{S} \tilde{\mathbf{E}}_i^n - \\
\sum_{f=1}^4 \left(k_e \mathbf{F}_{\Gamma_f} (\tilde{\mathbf{E}}_j^n - \tilde{\mathbf{E}}_i^n) + v_h \mathbf{G}_{\Gamma_f} (\tilde{\mathbf{H}}_j^{n-\frac{1}{2}} - \tilde{\mathbf{H}}_i^{n-\frac{1}{2}}) \right) \\
\varepsilon \mathbf{M} \frac{\tilde{\mathbf{E}}_i^{n+1} - \tilde{\mathbf{E}}_i^n}{\Delta t} &= \mathbf{S} \tilde{\mathbf{H}}_i^{n+\frac{1}{2}} + \\
\sum_{f=1}^4 \left(k_h \mathbf{F}_{\Gamma_f} (\tilde{\mathbf{H}}_j^{n+\frac{1}{2}} - \tilde{\mathbf{H}}_i^{n+\frac{1}{2}}) - v_e \mathbf{G}_{\Gamma_f} (\tilde{\mathbf{E}}_j^n - \tilde{\mathbf{E}}_i^n) \right),
\end{aligned} \quad (9)$$

where Δt is the size of time step, $\tilde{\mathbf{E}}$ and $\tilde{\mathbf{H}}$ differ by half a time step. Following the CFL condition, the maximum time step size is limited by the smallest element.

The size of the smallest and biggest element is always large in practice, so that the time step size is too short for most elements which leads to a huge number of time steps. The LTS-DGTD method in [2] is:

$$\begin{aligned}
\mu \mathbf{M} \frac{\tilde{\mathbf{H}}_i^{n+\frac{1}{2p}} - \tilde{\mathbf{H}}_i^{n-\frac{1}{2p}}}{\Delta t/p} &= -\mathbf{S} \tilde{\mathbf{E}}_i^n - \\
\sum_{f=1}^4 \left(k_e \mathbf{F}_{\Gamma_f} (\tilde{\mathbf{E}}_j^n - \tilde{\mathbf{E}}_i^n) + v_h \mathbf{G}_{\Gamma_f} (\tilde{\mathbf{H}}_j^{n-\frac{1}{2}} - \tilde{\mathbf{H}}_i^{n-\frac{1}{2}}) \right) \\
\varepsilon \mathbf{M} \frac{\tilde{\mathbf{E}}_i^{n+\frac{1}{p}} - \tilde{\mathbf{E}}_i^n}{\Delta t/p} &= \mathbf{S} \tilde{\mathbf{H}}_i^{n+\frac{1}{2p}} + \\
\sum_{f=1}^4 \left(k_h \mathbf{F}_{\Gamma_f} (\tilde{\mathbf{H}}_j^{n+\frac{1}{2p}} - \tilde{\mathbf{H}}_i^{n+\frac{1}{2p}}) - v_e \mathbf{G}_{\Gamma_f} (\tilde{\mathbf{E}}_j^n - \tilde{\mathbf{E}}_i^n) \right),
\end{aligned} \quad (10)$$

in which $p = 3^{M-N}$, M is the number of levels and N is the level of i . The minimum element size between levels varies by three times and the time step size is three times either. This greatly reduces the total amount of calculation. However, this scheme has a higher error in 3D space than in 2D space, so that the interpolation method is used on the different time step fields between adjacent elements of different levels to obtain pseudo time steps.

This paper uses an interpolation method as follows:

$$\mathbf{u}_i^{n+T_j} = \frac{\Delta t_j}{\Delta t_i} (\mathbf{u}_i^n - \mathbf{u}_i^{n-T_i}), \quad (11)$$

where u is field and T_j is the time step size of element j , T_i is the time step size of element i . The computation work is shown in Fig. 1. The ratio of time step sizes of level1, level2 and level3 is 1:3:9. Pseudo time steps of higher level are obtained by equation (11) and provided to lower level, the stability of this scheme is proven in [1]. Obviously, the acceleration of LTS is determined by M and the number of elements in different levels.

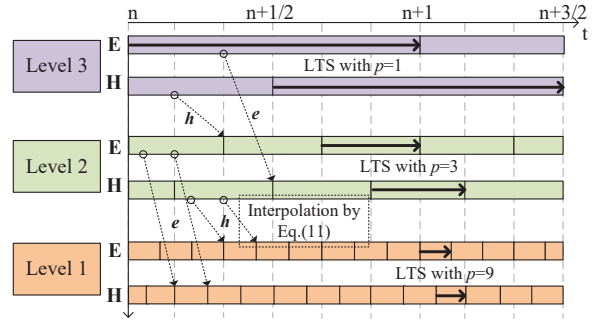


Fig. 1. Computation work of LTS-DGTD with interpolation, \mathbf{E} and \mathbf{H} are pseudo electric and magnetic field obtained by equation (11), respectively.

III. THE MINIMUM ROUNDTRIP STRATEGY FOR LTS-DGTD

Thread-level LTS-DGTD parallelism is very easy to implement due to the independence of the element in equation (10). When updating the electric and magnetic fields, it only depends on the fields of i and j in the previous time step. As for processor-level parallelism, equation (10) can be written as:

$$\begin{aligned}
\mu \mathbf{M} \frac{\tilde{\mathbf{H}}_i^{n+\frac{1}{2p}} - \tilde{\mathbf{H}}_i^{n-\frac{1}{2p}}}{\Delta t/p} &= -\mathbf{S} \tilde{\mathbf{E}}_i^n - \\
\sum_{f=1}^x \left(k_e \mathbf{F}_{\Gamma_f} (\tilde{\mathbf{E}}_j^n - \tilde{\mathbf{E}}_i^n) + v_h \mathbf{G}_{\Gamma_f} (\tilde{\mathbf{H}}_j^{n-\frac{1}{2p}} - \tilde{\mathbf{H}}_i^{n-\frac{1}{2p}}) \right) - \\
\sum_{g=1}^y \left(k_e \mathbf{F}_{\Gamma_g} (\tilde{\mathbf{E}}_j^n - \tilde{\mathbf{E}}_i^n) + v_h \mathbf{G}_{\Gamma_g} (\tilde{\mathbf{H}}_j^{n-\frac{1}{2p}} - \tilde{\mathbf{H}}_i^{n-\frac{1}{2p}}) \right) \\
\varepsilon \mathbf{M} \frac{\tilde{\mathbf{E}}_i^{n+\frac{1}{p}} - \tilde{\mathbf{E}}_i^n}{\Delta t/p} &= \mathbf{S} \tilde{\mathbf{H}}_i^{n+\frac{1}{2p}} + \\
\sum_{f=1}^x \left(k_h \mathbf{F}_{\Gamma_f} (\tilde{\mathbf{H}}_j^{n+\frac{1}{2p}} - \tilde{\mathbf{H}}_i^{n+\frac{1}{2p}}) - v_e \mathbf{G}_{\Gamma_f} (\tilde{\mathbf{E}}_j^n - \tilde{\mathbf{E}}_i^n) \right) + \\
\sum_{g=1}^y \left(k_h \mathbf{F}_{\Gamma_g} (\tilde{\mathbf{H}}_j^{n+\frac{1}{2p}} - \tilde{\mathbf{H}}_i^{n+\frac{1}{2p}}) - v_e \mathbf{G}_{\Gamma_g} (\tilde{\mathbf{E}}_j^n - \tilde{\mathbf{E}}_i^n) \right)
\end{aligned} \quad (12)$$

where x is the number of elements belong to the local processor and y is the number of elements belong to adjacent processors. Γ_g is the boundary adjacent with another processor.

When the LTS-DGTD method executing on a distributed platform, the communication is performed between the adjacent processors which always are defined on a host core of nodes. In this paper, the message passing interface (MPI) is used to support the communication between nodes. The logP [24] model is the most popular topology of distributed platforms, and its structure is shown in Fig. 2.

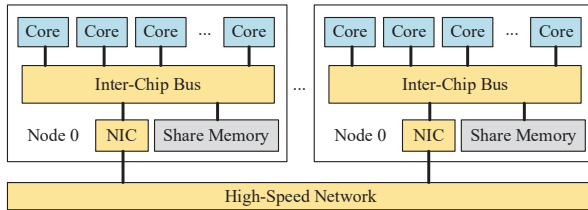


Fig. 2. The structure of massively distributed platform. Processor is defined on cores, and NIC is the network interface controller.

The running time of the logP model is:

$$T = T_c + T_m, \tag{13}$$

where T_c is the time of calculation, T_m is the time of communication. The computational time complexity of LTS-DGTD in each iteration step is determined by the number of elements of LTS levels. Communication time complexity T_m can be expressed as

$$T_m = \sum_{n=1}^R \frac{P_n}{S_n}, \tag{14}$$

where S_n is the network bandwidth, R is the number of roundtrips between nodes and P_n is the amount of data transmission per roundtrip. S_n can be considered a constant when data transmitting continuously between nodes. The memory of each node is accessed locally for the storage structure of the logP model, non-dependent processors do not influence each other while communicating, thus they can communicate at the same time. We should select nodes that communicating at the same time to reduce the number of roundtrips, so a minimum number of roundtrip (MNR) strategy is proposed to solve this problem.

As the global graph shown in Fig. 3, the number in a node represents the rank of a processor, the edge indicates the communication between two processes. Obviously, simple graph sorting cannot obtain the MNR. Referring to the Kruskal algorithm [29], only each independent subtree is saved in the process while finding the

minimum spanning tree (MST), the number of independent subtrees is the MNR. This algorithm for finding MNR of the LTS method is MNR-LTS algorithm which has four steps as follows.

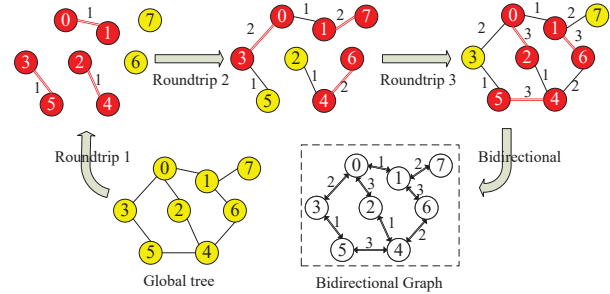


Fig. 3. The minimum number of roundtrips strategy and the graph of communication. The weight of edge is its roundtrip among the communication, the red circles indicate that the processor communicates in this roundtrip and the yellow circles indicate that the processor does not communicate.

Step 1 Mark the weights of edges in the graph as 0, set the current roundtrip as 1.

Step 2 Pick all unconnected edges in the graph, remark the weight of those edges as current roundtrip.

Step 3 Remove the picked edges of the previous step and create a new graph, add one to current roundtrip.

Step 4 Repeat steps 2 and 3 until all edges are remarked. These four steps are performed in every LTS levels, sum of all LTS levels roundtrip is the final number of roundtrips. The weight of an edge is the roundtrip of the communication between the processors connected by this edge. Since this graph is a bipartite graph above send and receive, the MNR should be twice the current roundtrip. Because the graph topology of nodes exists naturally, this method can be used on most distributed computers, such as distributed computing systems and supercomputers.

IV. PARALLELISM ON SUNWAY SUPERCOMPUTERS

The most classic Sunway many-core CPU is SW26010, which is based on the Alpha framework and composed of four core groups (CG). Each CG contains a management processing (MPE) and an 8×8 CPE cluster. Each CG has 8G of share memory space and can be accessed by the primary and secondary cores, while each CPE core has a separate LDM sized 64KB. The CPE core reads the LDM quickly, but because the local memory space is too small, it needs to communicate with the host memory using the direct memory access (DMA).

The task division of inner-chip is important for Sunway manycore CPU. The structure of Sunway CPU is

shown in Fig. 4, MPE broadcast the tetrahedrons and matrices to CPEs, and LDM receives them. However, the bandwidth of the interface is not optimal thus the communication between MPE and CPEs is slow. The conventional method to solve this problem is using DMA to transmit data. On the new general Sunway supercomputer, there is a better method to improve the communication efficiency of MPE to CPEs.

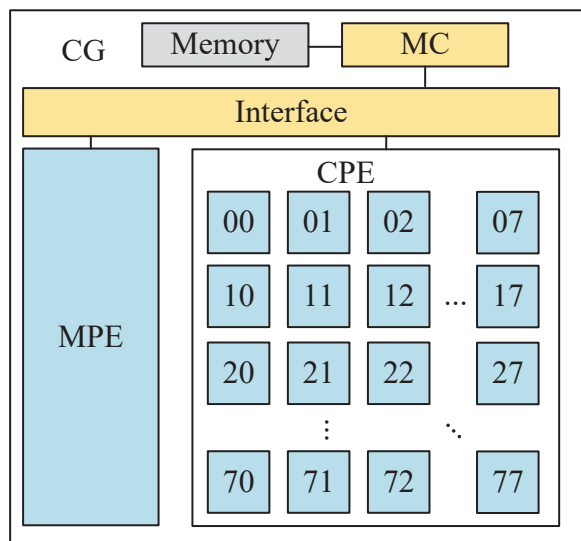


Fig. 4. Structure of SW26010 and new general Sunway CPU.

When LDM transmits data, MPE uses DMA channel to transfer data from main memory to local memory, which is suspended from the core processor and allows access to parts of local memory that are not data transferred for operation. At the RMA double-buffer (RMA-DB) strategy, the received CPE memory buffers are divided into two parts when transferring data from one core to another through CPE inter-communication on CPEs. The two buffers are used to transfer and calculate data alternately to achieve the effect of communication masking, which hides the transmit time behind the computation time as Fig. 5 shows. At the same time, the application of MNR strategy to control process-level data exchange between the core groups improves the parallel efficiency and is suitable for large-scale parallel computing.

It should be noted that although the RMA-DB strategy can hide the communication time behind the calculation time, the MPE to LDM still consumes a lot of time, which is caused by the Sunway CPU architecture.

V. NUMERICAL RESULTS AND ANALYSIS

Firstly, a radiation problem is considered to test the LTS-DGTD method with RMA-DB strategy. Patch

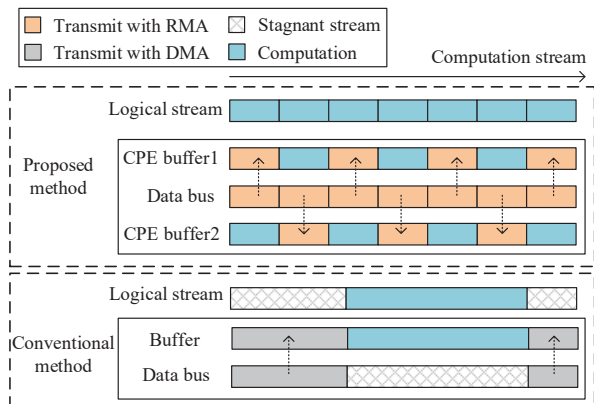


Fig. 5. Transmit data by RMA and DMA. In proposed method, buffer 1 and buffer 2 transfer data using RMA alternately. The stagnant stream denotes there is nothing to do at that moment.

Table 1: Running time of the proposed method

Kernel	LTS level	MPE time(s)	CPEs Cluster time(s)	RMA-DB time(s)
Update E	Level1	263.1	148.2	81.4
	Level2	295.5	156.3	85.2
	Level3	1845.6	945.8	443.7
Update H	Level1	262.5	147.8	80.9
	Level2	296.0	155.2	86.8
	Level3	1845.2	946.1	443.3

antennas are widely used in mobile communication and miniaturized radars, so in this paper a rectangular patch antenna is used to demonstrate the accuracy and efficiency of the proposed method. The rectangular patch is $22.7091 \text{ mm} \times 30.1615 \text{ mm}$, treated as perfect electric conductor (PEC), the size of the dielectric substrate is $34.92 \text{ mm} \times 38.65 \text{ mm} \times 3 \text{ mm}$ and its relative permittivity is 4.5. A modulated Gaussian pulse in 2GHz to 6 GHz excites the coaxial wave port at the bottom of the antenna, inner and outer radius of the coaxial line are 0.44 mm and 1.5 mm, respectively. The coaxial line makes the antenna mesh has multi-scale size, there is no sparse matrix solver that can use RMA-DB strategy on the new sunway supercomputer for the time being, thus, the LTS-DGTD method is suitable for this problem. According to the wavelength of 4 GHz, 52,755 tetrahedrons were obtained through meshes discretisation, which is partitioned into 3 LTS levels in LTS-DGTD, the time step sizes are from 0.0602 ps to 0.5418 ps. The geometry and mesh of the patch antenna are shown in Fig. 6.

The S-parameter of the LTS-DGTD method on CPU and Sunway processor are exhibited in Fig. 7, the result

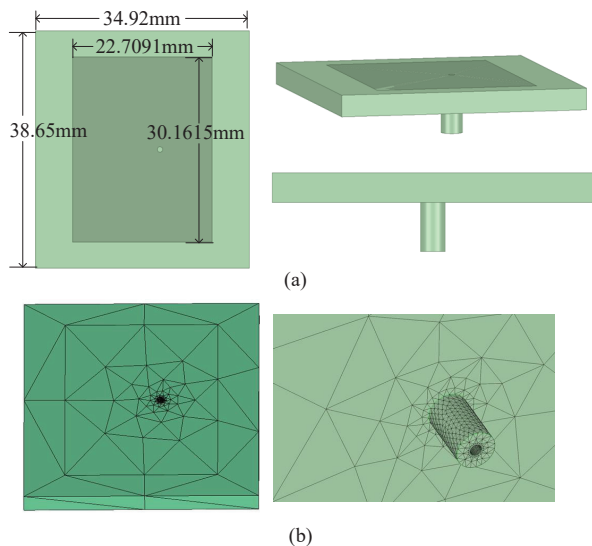


Fig. 6. The model and mesh of patch antenna. (a) Front, top, and side views of the model; (b) Top and bottom meshes.

of commercial software Ansys-HFSS is also proposed in Fig. 7. Its obviously that the accuracy of the proposed method on CPU is similar to that on Sunway. To show the efficiency of the RMA-DB strategy, the running time of different parts of the proposed method is summarized in Table 1, the update E is the first stage of Eq. (12) and the update H is the second stage of Eq. (12). With the RMA-DB strategy, CPEs has 4.15 acceleration than MPE, that demonstrates the efficiency of the RMA-DB strategy.

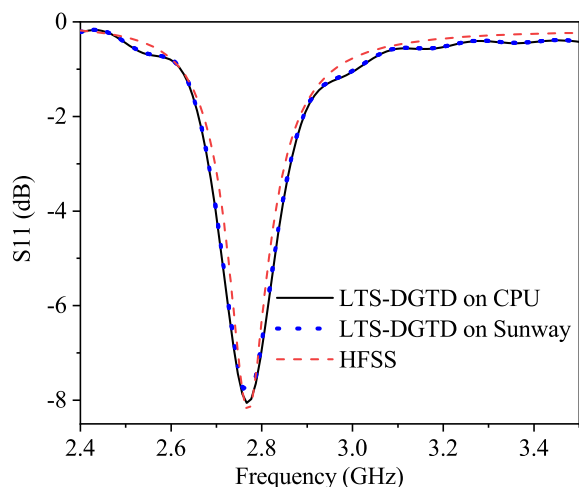


Fig. 7. Transmit data by RMA and DMA. In proposed method, buffer 1 and buffer 2 transfer data using RMA alternately. The stagnant stream denotes there is nothing to do at that moment.

Secondly, a slot antenna is used to demonstrate the performance of MNR strategy on homogeneous distributed computers. The geometry of the antenna is shown in Fig. 8. This antenna is excited by a coaxial wave port with the modulated Gaussian pulse in 15 GHz to 17 GHz. The antenna model is discretized into 1101096 tetrahedrons and is simulated by the DGTD-LTS method with MNR strategy on a homogeneous distributed computer. The homogeneous computer has 16 nodes, each node has 72 cores (Intel Xeon Gold 6140 @ 2.30GHz). The 120, 360, 720 and 936 cores cases employ 2, 6, 12 and 13 nodes, respectively. Cores are executed as threads by OpenMP. The Fig. 9 shows the gain obtained by the MNR strategy and the FDTD method. The calculation details of the original method and MNR strategy are given in Table 2. Compared with the original method, the MNR strategy significantly improves computational efficiency, and as the number of nodes increases, the acceleration becomes more obvious.

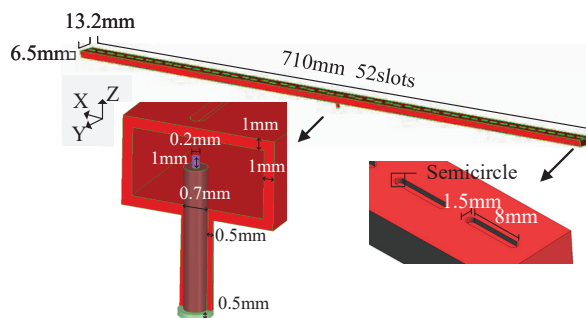


Fig. 8. Geometry of the slot antenna.

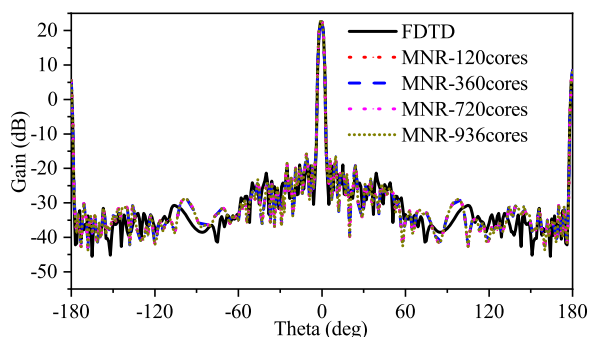


Fig. 9. Gain of the slot antenna obtained by the MNR strategy and FDTD method.

To show the performance of MNR strategy on super-computers, a scatter analysis of an automobile is considered. The analysis of radar scattering can be regarded as a typical case of the electrically large-scale target simulation, similar analysis can be aimed at aircrafts, ships

Table 2: Computational Performance of the slot antenna

Number of cores	Time of original (min)	Time of MNR (min)	Speedup
120	143.07	136.55	1.05
360	56.95	47.44	1.20
720	34.10	24.75	1.38
936	29.07	19.67	1.48

Table 3: Computational Performance of automobile

Method	Number of Roundtrips	Time (s)	Speedup
Original	7590	8895.6	1
MNR	341	354.1	25.1

and other targets. The size of the automobile is $5.20 \text{ m} \times 1.82 \text{ m} \times 1.55 \text{ m}$, for the convenience of calculation, the shell of the car is regarded as PEC, the interior of the car is vacuum, and the tire is non-conductive rubber, which is regarded as microwave absorbing material. The plane wave with frequency of 800 MHz to 1200 MHz illuminates the car from front to back. Waves with this frequency band can attenuate slowly and propagate to distant place. To prove the efficiency of MNR strategy in the case of multiple nodes, this example is simulated by the Sunway TaihuLight supercomputer. The Sunway TaihuLight supercomputer has 4 SW26010 CPU per node and the SW26010 CPU has 65 cores [26].

The model is divided into 3,188,485 tetrahedrons and the LTS-DGTD method simulates this model with 1600 nodes (6400 processors) on the Sunway TaihuLight supercomputer. To confirm the accuracy of the proposed method, the results of using and not using MNR strategy are compared and shown in Fig. 10. The normalized electric fields of the automobile from 3 ns to 14 ns obtained by the proposed method are shown in Fig. 11. In order to analyze the performance of MNR strategy, the calculation details are given in Table 3. Its obviously that the MNR strategy reduces the number of roundtrips by 22.3 times and improves the speed of data transmission by 25.1 times, and this result verifies the effectiveness of MNR strategy.

Slot antenna array always have high working frequency and strongly resonance, its transient characteristic is hard to be simulated by classical numerical method. There a slot antenna array to highlight the validity of the two proposed methods is shown. The array size is $0.34115 \text{ m} \times 0.018477 \text{ m} \times 0.35456 \text{ m}$ and its working frequency band is 15.9 GHz–17.9 GHz, the curved slots make the model have multi-scale characteristics. Absorb boundary condition (ABC) is used to terminate the air box. A modulated Gaussian pulse from 14 GHz

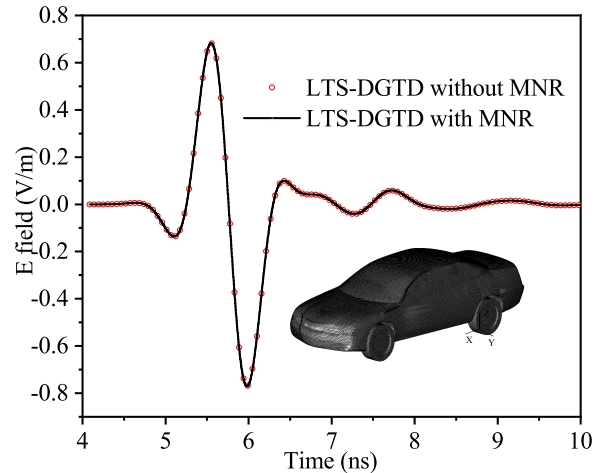


Fig. 10. Comparisons of electric field between the LTS-DGTD method with and without the MNR strategy.

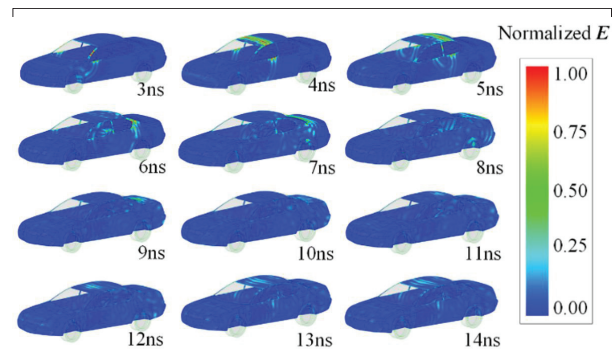


Fig. 11. Normalized electric field of the automobile from 3 ns to 14 ns proposed by the LTS-DGTD method with MNR strategy.

to 19 GHz is applied into a coaxial port which loaded at the bottom of the array. The model is divided into 19,320,201 tetrahedrons, whose number of unknowns is 386,404,020. The proposed method partitions the mesh into 5 LTS levels and the time steps are from 0.0243 ps to 1.9683 ps.

The proposed method is executed with 4000 nodes (4 processors per node) on the new Sunway supercomputer, Fig. 12 shows the normalized directivity of 16GHz provided by measurement and the proposed method in plane yoz, and Fig. 13 shows the 3D directivity of the array and its transient electric fields at 1.5ns, 2ns and 3ns, which is helpful for us to analyze the excitation mode and design of slot antennas. The iteration time and strong scalability efficiency are presented in Table 4. The results show that the proposed method can achieve 73.8% parallel efficiency [24] when extended to 1040000 cores of 16000 processes, which expands the scale of the LTS-DGTD

Table 4: Computational Performance of automobile

Number of procs	Number of cores	Time of update (s)	Efficiency
1600	104,000	809.5	100.0
3200	208,000	409.8	98.7
6400	416,000	225.1	89.9
16000	1,040,000	109.6	73.8

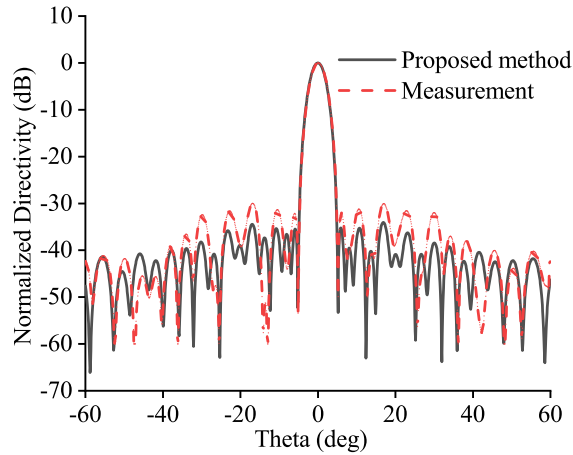


Fig. 12. Normalized directivity of slot antenna array in plane yoz.

method from hundreds of nodes to tens of thousands of nodes, and can effectively support its operation on modern supercomputers.

VI. CONCLUSION

In this paper, a high-performance parallelism of the LTS-DGTD method on China's homegrown Sunway supercomputers is proposed for the transient electromagnetic analysis. The MNR strategy is applied to reduce the communication roundtrip between multi-nodes system for the LTS-DGTD method, and a newly double-buffer strategy is employed to make the communication overlapped computation in CPEs with RMA transmission. Several numerical examples are used to demonstrate the performance and efficiency of the proposed method, which include the transient simulation of automobile, antenna and antenna array with analyzed on the Sunway TaihuLight and the new Sunway supercomputer. Numerical results show the parallel efficiency of the proposed method is 73.8% from 1600 nodes to 16000 nodes, which can be quite important for the application of the LTS-DGTD method in industrial simulation. At the same time, the MNR strategy in the proposed method can also be used on multi-node supercomputers other than Sunway supercomputer.

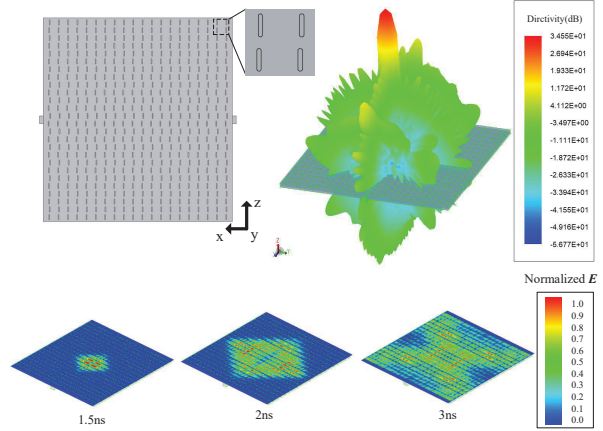


Fig. 13. Normalized directivity of slot antenna array in plane yoz.

ACKNOWLEDGMENT

The authors would like to thank Dr. Shugang Jiang from Xidian University for his valuable suggestions for this article. They would also like to appreciate constructive and professional comments from Editors and anonymous reviewers. This work was supported by the National Science Foundation of China (Grant No. 61901323), the Key Research and Development Program of Shaanxi (2021GXLH-02, 2022ZDLGY02-02) and the Fundamental Research Funds for the Central Universities (QTZX22155).

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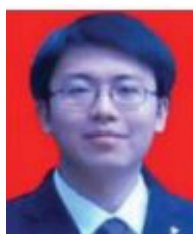
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