

# Super-Broadband Rectifier with Wide-band Resistance Compression Network and Harmonic Cycling for RF-Harvesting

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**Abstract** – In this paper, a super-broadband (SBB) rectifier using a wideband resistance compression network (WRCN) and harmonic cycling is proposed, simulated, fabricated, measured and analyzed in detail for the harvesting of ambient radio frequency (RF) energy. Meanwhile, impedance compression and matching are achieved to implement the SBB using WRCN and impedance operation networks. Additionally, harmonic cycling structure and bending technology are employed to improve the power conversion efficiency (PCE) and reduce the size, respectively. For demonstration, a prototype of the proposed rectifier is fabricated and measured. The measured results are in good accordance with the simulated ones, indicating that the rectifier can provide high efficiency and ultra-broadband rectification characteristics. A PCE over 50% is realized at 3.5 GHz with an input power range of 6–24 dBm, and a PCE of 75% is obtained at an input power of 18 dBm. The PCE is greater than 50% at 17 dBm with an input frequency of 2.7–4.6 GHz. This work can find significant applications in the development of RF-harvesting.

**Index Terms** – bending technique, harmonic cycling, RF-harvest, super-Broadband rectifier, wide-band resistance compression technique.

## I. INTRODUCTION

With the rapid development of communication technologies, human beings' living surroundings are full of electromagnetic waves. If these electromagnetic energies can be recycled and harvested on the spot, we can get rid of the limitation that their batteries determine the lifetime of electronic devices. Consequently, radio frequency (RF)-harvest is currently attracting much

attention in scientific and industrial fields. Various RF-harvest devices are currently used in the medical field, smart homes, electric vehicles, consumer electronics, and drone charging [1]. Many rectifiers can now achieve high power conversion efficiency (PCE) in narrow band ranges. However, with the rise of 5G and Internet of Things (IoT) technologies and MIMO radars [2], wider bands are being used for wireless communications where the electromagnetic energy is distributed across multiple bands. Therefore, it is becoming increasingly important to design broadband rectifiers to maximize the amount of power that can be harvested [3, 4].

A lot of rectifiers have been reported to address these mentioned problems. A rectifier consisting of a two-stage coupler is proposed and discussed in [5], which allows the reflected power caused by impedance mismatch to be re-rectified, improving the rectification efficiency, and a fractional bandwidth of 21.5% and a PCE over 70% have been achieved from 2.08 GHz to 2.58 GHz. The rectifier in [6] uses a non-uniform transmission line to achieve broadband rectification characteristics, resulting in a PCE higher than 50% over a bandwidth of 0.4–1 GHz. In [7], a two-stage impedance matching network was used to achieve a PCE greater than 50% with a fractional bandwidth over 37% (1.8–2.72 GHz). In [8], by using a taper impedance matching network, a broadband rectifier is achieved over 2–3.05 GHz with an input power of 10 dBm, and a peak PCE of 75.8% is obtained at an input power of 14 dBm. There are other methods to increase the operating bandwidth of rectifiers by using sub-rectifiers operating in a different band range [9, 10]. In addition, the PCE can be improved by increasing the matching quality using varactor diodes and

MOSFETs given in [10, 11]. However, it is still a great challenge to design rectifiers to cover multiple frequency bands.

This paper proposes an ultra-broadband rectifier with a wideband resistance compression network (WRCN) and harmonic cycling for RF-harvesting to address this issue. Two branches are connected using WRCN to achieve wideband impedance matching. The PCE of the rectifier is further improved with broadband, and a harmonic cycling technique is considered to achieve a broadband high-efficiency rectifier. The proposed rectifier is designed to get a PCE greater than 50% at an input power of 17 dBm from 2.7 to 4.6 GHz, which has a fractional bandwidth over 65% and provides a peak PCE up to 75% at 3.5 GHz with an input power of 18 dBm.

## II. THEORETICAL ANALYSIS OF THE RECTIFIER

Figure 1 is the schematic diagram of the designed super-broadband (SBB) rectifier for RF energy harvesting applications using WRCN and harmonic cycling. The SBB rectifier circuit consists of two load resistors, a DC-pass filter (part A), two HSMS286C Schottky diodes, an impedance operating network (part B) and a wideband WRCN (part C).

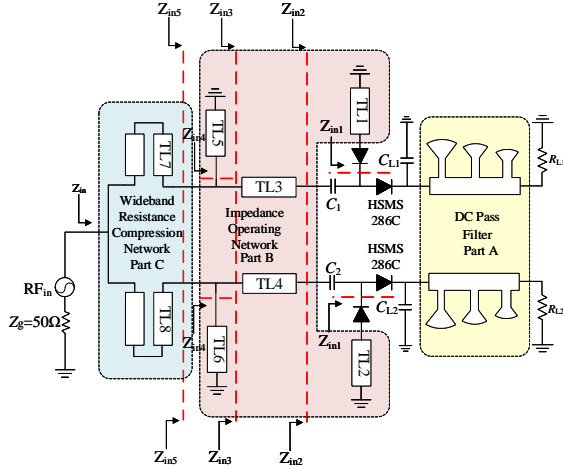


Fig. 1. Schematic of the proposed super-broadband rectifier.

### A. Design of the DC-pass filter and harmonic cycling

Since the Schottky diode is a non-linear component, it would generate fundamental frequency and high harmonics in the process of converting the RF signal to DC signal, while the high harmonics are mainly dominated by the second harmonic, and the rest of the high harmonics carry too little energy that can be negligible. In order to make the output voltage more stable, DC-pass filters

combine lumped and distributed elements in this design, which is to smooth the output DC waveform and return the fundamental and higher harmonics to the Schottky diode for re-rectification.

The harmonic cycling structure in the proposed broadband rectifier consists of three linear microstrip stubs and three fan-shaped microstrip stubs. As depicted in Fig. 2, a fan-shaped stub has two characteristic parameters: the radius  $r_1$  and the angle  $\alpha$ . The input impedance of the fan-shaped stub can be calculated from equations (1), (2), (3) and (4) [12]:

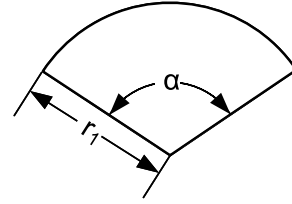


Fig. 2. Characteristic parameters of the fan-shaped stub.

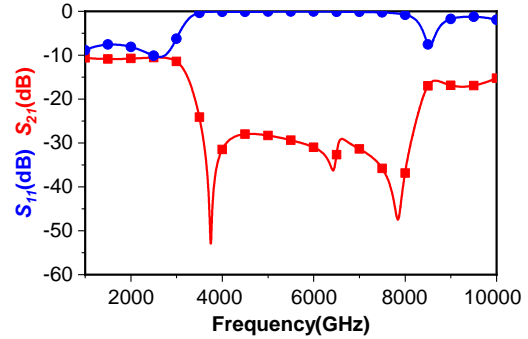


Fig. 3. The simulated S-parameters of harmonic cycling.

$$X_1 = \frac{h}{2\pi r_1} Z_0(r_1) \frac{360 \cos(\theta_1 - \varphi_2)}{a \sin(\varphi_1 - \varphi_2)}, \quad (1)$$

$$\tan \theta_1 = \frac{N_0(kr_1)}{J_0(kr_1)}, \tan \varphi_1 = \frac{J_1(kr_1)}{N_1(kr_1)}, (i = 1, 2), \quad (2)$$

$$Z_0(r_1) = \frac{120\pi [J_0^2(kr_1) + N_0^2(kr_1)]^{\frac{1}{2}}}{\sqrt{\epsilon_r} [J_1^2(kr_1) + N_1^2(kr_1)]^{\frac{1}{2}}}, \quad (3)$$

$$k = \frac{2\pi\sqrt{\epsilon_{re}}}{\lambda_0}, \quad (4)$$

where  $J_0(x)$ ,  $N_0(x)$ ,  $J_1(x)$ ,  $N_1(x)$  represent the first class of 0-order Bessel function, the second class of 0-order Bessel function, the first class of 1-order Bessel function and the second class of 1-order Bessel function, respectively.  $\lambda_0$  denotes the wavelength in free space,  $\epsilon_{re}$  is the

equivalent dielectric constant, and  $h$  is the thickness of the dielectric substrate. In addition, the resonance point of the input impedance of the fan-shaped stub is less affected by frequency variations than that of the linear stub. Thus, the smoother return loss  $S_{11}$  curve of the fan-shaped stub provides a broader bandwidth, which also exhibits a wider stop band in the DC-pass filter. Here, the DC-pass filter mainly consists of fan-shaped stubs and linear stubs, with the fan-shaped stubs to reduce the longitudinal size and the linear stubs to avoid the problem of the excessive transverse size of the fan-shaped stubs. The S-parameter is presented in Fig. 3, showing that the designed DC-pass filter can suppress the fundamental and higher harmonics of the RF signal and ensure a smooth DC output.

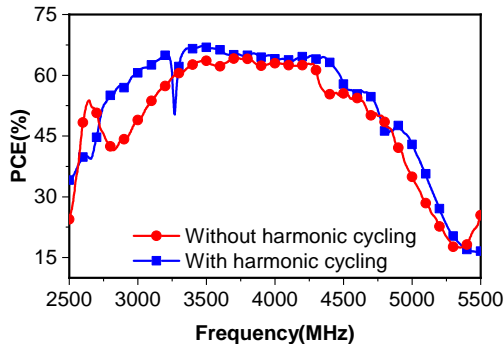


Fig. 4. Comparison of the PCE with and without the harmonic cycling structure.

A comparison of the PCE with and without harmonic loop structure at an input power of 15 dBm is shown in Fig. 4, where the DC-pass filter can recover fundamental and second harmonics over a wide frequency range and improve the PCE. Furthermore, since the filter will be integrated into the circuit, there will be inevitable interactions with the other structures. Therefore, the parameters of the DC-pass filter structure should be adjusted to be optimal for the entire rectifier circuit design.

### B. Design of an impedance operation network (ION)

In this design, an ION is used to convert the complex impedance  $Z_{in1}$  into a wide resistance  $Z_{in3}$ . The upper and lower branches in the ION have the same structures, which both consists of two short-circuit stubs TL1 (TL2), TL5 (TL6) and a section of microstrip transmission line TL3 (or TL4). Thus, the upper branch is used as an example to discuss the operating principle and parameters in this section.

Firstly, the upper branch of the ION consists of two short-circuit stubs TL1, TL5 and a section of microstrip transmission line TL3, where TL1 is mainly to counteract the capacitive characteristics carried by parallel

branch diodes. Since the diode is mainly capacitive in its operating range, TL1 is used as a short-circuit inductor to compensate for the capacitive characteristics of the diode in the operating band by connecting the inductive and capacitive in series. The characteristic impedance and electrical length of TL1 are  $Z_1$  and  $\theta_1$ , respectively. The input impedance of the diode in parallel is denoted as  $Z_{d1}=R_{d1}+jX_{d1}$ . Then, the input impedance of the branch after series connection with TL1 can be described as:

$$Z_{in1}(f) = R_d + jX_d + jZ_1 \tan \theta_1. \quad (5)$$

In order to better understand the design, we define the operating band as  $(f_1, f_2)$ , where  $f_1 < f_2$  and  $f_2/f_1=k$ , which can be further denoted as  $\theta(f_2)=k\theta(f_1)=\theta_1$ . Under ideal circumstances, TL1 should compensate for the capacitive characteristic of caused by the diodes in parallel branch with frequency ranging from  $f_1$  to  $f_2$ , and hence, the characteristic impedance and electrical length of TL1 for a specific power can be calculated using:

$$\text{Im}(Z_{in1}(f_1)) = -\text{Im}(Z_{in1}(f_2)). \quad (6)$$

The TL1 can reduce the input impedance variation of the two diodes in the operating bandwidth and provide a basis for further impedance compression. The diode used in this design is the HSMS286C, and we integrate two diodes into one package. After optimization in Advanced Design Simulation (ADS) with Harmonic Balance Simulation (HB), the characteristic impedance and electrical lengths of TL1(TL2) is calculated at 3.5 GHz to be  $Z_1=81 \Omega$ ,  $\theta_1=41.2$  deg. At an input power of 17 dBm, the input impedance  $Z_{in1}$  is shown in Fig. 5 after using the series short-circuit stub TL1(TL2), which is equivalent to an inductor, to cancel the diode capacitance.

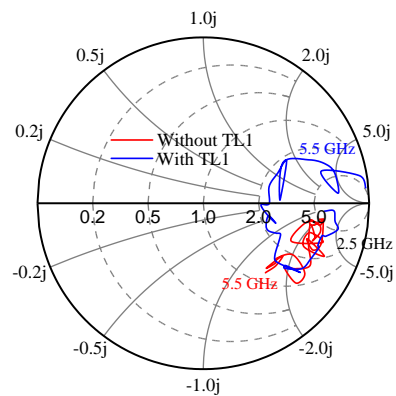


Fig. 5. Comparison of with and without TL1.

Secondly, the microstrip transmission line TL3 has the role of adjusting the imaginary part of the rectifier's input impedance  $Z_{in2}$  after TL1. To calculate the characteristic impedance  $Z_3$  and electrical length  $\theta_3$  of

the series microstrip transmission line TL3, the rectifier initial input impedance at  $f_1$  and  $f_2$  is expressed as  $Z_{in2}(f_1)=R_{d11}+jX_{d11}$  and  $Z_{in2}(f_2)=R_{d22}+jX_{d22}$ . Then, the rectifier input impedance at  $f_1$  and  $f_2$  after TL3 can be obtained and is given by equations (7) and (8):

$$Z_{in3}(f_1) = Z_3 \frac{Z_{in2}(f_1) + jZ_3 \tan \theta_3(f_1)}{Z_3 + j(Z_{in2}(f_1)) \tan \theta_3(f_1)}, \quad (7)$$

$$Z_{in3}(f_2) = Z_3 \frac{Z_{in2}(f_2) + jZ_3 \tan \theta_3(f_2)}{Z_3 + j(Z_{in2}(f_2)) \tan \theta_3(f_2)}. \quad (8)$$

The characteristic impedance and electrical length of TL3(TL4) were calculated to be  $Z_4=77 \Omega$ ,  $\theta_3=153$  deg at 3.5 GHz.  $Z_{in2}(f_1)$  and  $Z_{in2}(f_2)$  in the equations can be obtained using ADS simulation. Figure 6 shows the input impedance  $Z_{in3}$  of the rectifier in the 2.5–5.5 GHz band. It is observed that at an input power of 17 dBm, the real part of  $Z_{in3}$  in the frequency band of interest is approximately 39–50  $\Omega$ , and the imaginary part nearly oddly symmetrical about the 3.5 GHz frequency. In addition, a bending technique has been adopted in this design, which greatly reduces the space occupied by the TL3, saving space and reducing manufacturing costs.

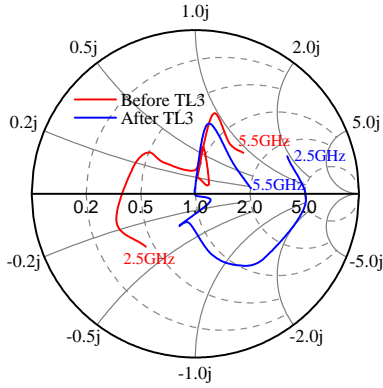


Fig. 6. Comparison of before and after TL3.

Thirdly, the input impedance of the rectifier is further compressed by TL5, which compresses the complex impedance into a wide resistance. Calculating the electrical length  $\theta_5$  and characteristic impedance  $Z_5$  of TL5, the inductance of the rectifier input impedance  $Z_{in3}$  at  $f_1$  and  $f_2$  is expressed as  $G_{in3}-jB_{in3}$ ,  $G_{in3}+jB_{in3}$ , respectively. Then, the inductance at  $f_1$  and  $f_2$  after TL5 is expressed as:

$$Y_{in4}(f_1) = \frac{1}{jZ_5 \tan \theta_5} = jB_{in3}, \quad (9)$$

$$Y_{in4}(f_2) = \frac{1}{jZ_5 \tan \theta_5} = -jB_{in3}. \quad (10)$$

The characteristic impedance and electrical length of TL5(TL6) were calculated to be  $Z_4=77 \Omega$ ,  $\theta_3=79.7$  deg at 3.5 GHz. Combining the two above equations gives the characteristic impedance and electrical

length of TL5. Further compression is applied to the input impedance to get oddly symmetric about the resistance axis. Compared to the graph before compression, the compressed input impedance only varies around the resistive axis of the Smith chart. It is worth noting that the proposed ION can also work over a wide range of input powers since the input impedance of a Schottky diode rectifier varies with the input power and has a similar trend in the bandwidth.

### C. Design of a WRCN

In this section, a WRCN is used to achieve impedance matching of the rectifier over broadband. The precondition for using WRCN is that the rectifier should have two branches. The principle behind it lies in the use of two transmission lines with electrical lengths of  $90^\circ+\Delta\theta$  and  $90^\circ-\Delta\theta$ , respectively, which can reduce the fluctuation of the input impedance due to load changes when it is connected in parallel. Compared to impedance compression networks, RCN requires additional ION, and impedance manipulation networks can transform complex impedances into wide resistances over a wide frequency range to a more stable achieve impedance matching over broadband.

The idea of designing the WRCN is presented as follows. Firstly, the WRCN should provide a resistor in the broadband, which is obtained from the previous ION analysis. For a conventional microstrip linear resistive compression network, it is difficult for the two branches to maintain complementary electrical lengths in the broadband, which can be well solved by using a double coupled line. Let the coupled line TL7 have an even-mode (odd-mode) characteristic impedance of  $Z_e$  ( $Z_o$ ) and an electrical length of  $\theta_{c1}$  at  $f_1$  and  $\theta_{c1}$  at  $f_2$ . Regarding the coupled line as a section of the transmission line, the characteristic impedance of this transmission line is  $Z_{eq}$ , while the electrical lengths at  $f_1$  and  $f_2$  are  $\theta_{eq1}$  and  $\theta_{eq2}$ , respectively. To achieve complementarity of electrical lengths,  $\theta_{eq1}$  and  $\theta_{eq2}$  should satisfy:

$$\theta_{eq1} + \theta_{eq2} = 180^\circ. \quad (11)$$

Then, the ABCD transmission matrix of the coupled line at  $f_1$  is modeled as equations (12), (13) and (14):

$$\frac{Z_e - Z_o \tan^2 \theta_{c1}}{Z_e + Z_o \tan^2 \theta_{c1}} = \cos \theta_{eq1}, \quad (12)$$

$$\frac{2Z_e Z_o j \tan \theta_{c1}}{Z_e + Z_o \tan^2 \theta_{c1}} = jZ_{eq} \sin \theta_{eq1}, \quad (13)$$

$$\frac{2j \tan \theta_{c1}}{Z_e + Z_o \tan^2 \theta_{c1}} = j \frac{\sin \theta_{eq1}}{Z_{eq}}. \quad (14)$$

Similarly, the equivalent ABCD transmission matrix of the coupling line at  $f_2$  can be obtained. The characteristic impedance and electrical lengths for the coupled line can be calculated using the above four equations, where the electrical lengths operating at  $f_1$  and  $f_2$  have a

relationship of  $\theta_{c2}=k\times\theta_{c1}$ . The characteristic impedance and electrical length for TL6 can be obtained using the same analysis, except that the equivalent electrical length of TL6 at  $f_1$  is  $\theta_{eq2}$  that equals to  $(180^\circ-\theta_{eq1})$ , and the equivalent electrical length at  $f_2$  is  $\theta_{eq1}$ . In addition, the parallel impedance of the two branches is  $50\Omega$ , which matches the source impedance.

### III. IMPLEMENTATION AND MEASUREMENT RESULTS

Based on the above principle analysis, the layout of the proposed rectifier is modelled in ADS and jointly optimized, which is shown in Fig. 7. The rectifier is printed on a F4B ( $\epsilon_{re}=2.55$ ,  $\tan\delta=0.002$ ) dielectric substrate with thickness of  $h=0.762\text{ mm}$  and a total size of  $94\times 60\text{ mm}^2$ . Herein, two HSMS2862C are used as rectifier diodes, and the capacitors are all Murata's GRM18 series 100 pf capacitors, and the load resistance is  $650\Omega$ . To facilitate adjustment, two experimental resistor boxes are used in the test. Alternatively, if it was preferred to use only one load, the resistance value of the replacement load should be twice the resistance value of the initial load, and the PCE would remain almost unchanged.

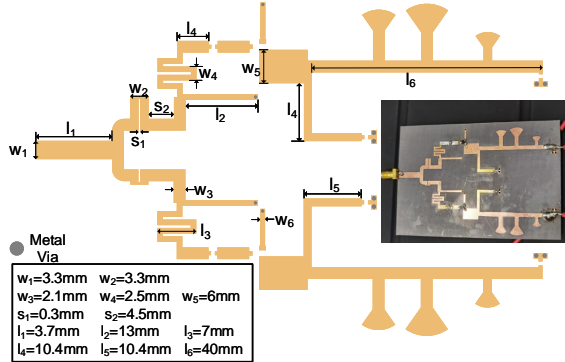


Fig. 7. Layout of the proposed rectifier.

In the experiment, an Agilent PNA-X vector network analyzer is used as a signal source, two adjustable resistor boxes are used as load resistors, and a multimeter is used to measure the output voltage. The proposed ultra-broadband rectifier is analyzed, fabricated and tested. Figure 8 gives a comparison of the simulated  $S_{11}$  of the proposed rectifier with the measured results at an input power of 17 dBm, showing that the rectifier has a good broadband characteristic. Herein, the PCE is calculated using equation (15) [13, 14]:

$$PCE(\%) = \frac{P_{DC}}{P_{RF}} = \frac{V_{out1}^2 + V_{out2}^2}{R_L \cdot P_{RF}}. \quad (15)$$

Figure 9 presents the simulated PCE versus measured PCE for input powers at 5 dBm, 10 dBm, 17 dBm, 20 dBm, respectively. From the results, we found that

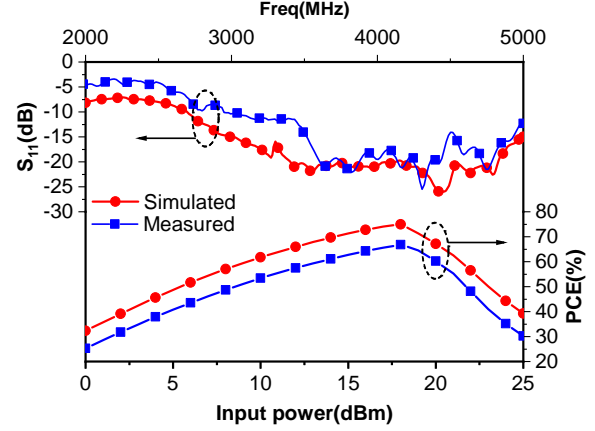


Fig. 8. (Upper lines) Measured and simulated  $S_{11}$  of the rectifier. (Lower lines) Measured and simulated PCE versus input power at 3.5 GHz.

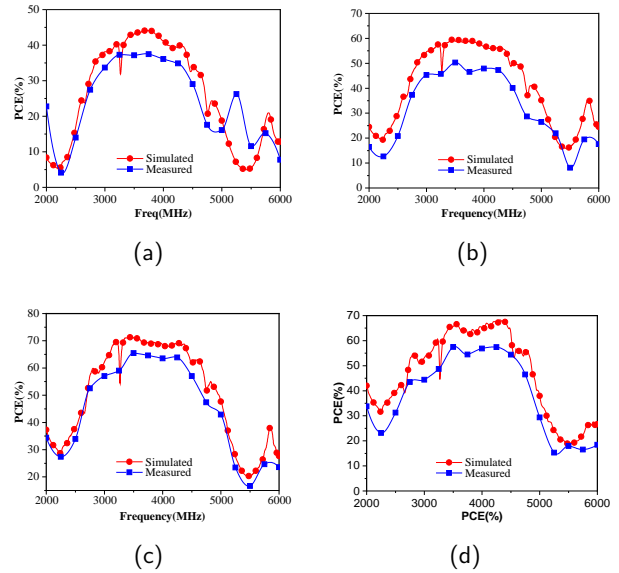


Fig. 9. Measured and simulated PCE variations at different input power levels (a) 5 dBm, (b) 10 dBm, (c) 17 dBm, and (d) 20 dBm.

Table 1: Comparison between the suggested rectifier and related designs

Ref.	Freq.(GHz)	FBW.	Max-PCE	Size( $\text{mm}^2$ )
[5]	2.08–2.58	20.8%	80.8%	$126\times 68$
[8]	2–3.05	41.5%	75.8%	—
[15]	0.915	—	74.2%	—
[16]	1.7–2.9	50%	76%	$56\times 36$
This work	2.7–4.6	52%	75%	$94\times 60$

there is a maximum band range of 2.7–5 GHz at an input power of 17 dBm with  $PCE>50\%$ .



Figure 8 shows the simulated and measured PCE variation with input power at a frequency of 3.5 GHz. We can see that the maximum conversion efficiency of 77% is obtained when the input power is 19 dBm, and a PCE > 50% is achieved with an input power of 6-24 dBm. Table 1 shows a comparison between the proposed rectifier and some previous similar works. The proposed rectifier has the widest bandwidth and balanced PCE. The difference between the experimental and simulated results is mainly caused by soldering errors and insertion losses of the SMA connectors.

#### IV. CONCLUSION

A super-broadband rectifier using a WRCN and harmonic cycling is proposed for RF-harvesting. Impedance matching over a wide bandwidth is achieved by using an impedance operation network consisting of three microstrip lines and a WRCN designed via coupled lines. The harmonic cycling structure further improves the PCE of the rectifier, while the bending technique is used to reduce the size of the rectifier. The proposed rectifier achieves a PCE over 50% from 2.7-4.6 GHz at an input power of 17 dBm, and the designed rectifier has a fractional bandwidth of over 50%. The techniques described in this work can also apply to other rectifier circuits.

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