A Novel GaN Power Amplifier Based on Quasi-Monolithic Microwave Integrated Circuits

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Abstract – In this paper, we propose a compact quasi-monolithic microwave integrated circuit (MMIC) ultra-wideband gallium nitride (GaN) power amplifier (PA), highlighting its innovative design approach and the associated fabrication techniques aimed at enhancing integration and performance. The discrete transistor is manufactured by a 0.35-μm GaN high electron mobility transistor (HEMT) process. The input matching network employs a GaAs passive device process for compact and wideband flexible design. The output matching network employs a ceramic technology for high power and low insertion loss design. The discrete transistor is connected to the input and output network with gold bonding wires. The PA exhibited a gain of 11 dB, a saturation power of 48 dBm, and a peak power-added efficiency of 32.8%.

Index Terms – Gallium nitride (GaN), matching network, monolithic microwave integrated circuit (MMIC), power amplifier (PA), ultra-wideband.

I. INTRODUCTION

Broadband power amplifier (PA) monolithic microwave integrated circuits (MMICs) are extensively studied and applied in electronic systems such as electronic countermeasure and multifunction platforms [1–4]. The key performance metrics, including the output power (P_{out}) and power-added efficiency (PAE), can critically impact the overall effectiveness of these systems [5–8]. The gallium nitride high electron mobility transistors (GaN HEMTs) on silicon carbide (SiC) substrates can offer notable advantages in radio-frequency (RF) applications, including the high breakdown voltage, superior current handling capability, and elevated power density [9]. Consequently, numerous high-power and high-efficiency GaN-based PAs have been proposed [10, 11]. To enhance their performance, a variety of advanced techniques have been developed, such as stacked field effect transistor (FET) technology [12], reactive filter synthesis, and asymmetric magnetically coupled resonator (MCR) technology [13].

Distributed amplifiers (DAs) have attracted considerable interest due to their excellent return loss and wide bandwidth characteristics [14]. By incorporating the parasitic capacitance of multiple transistors into artificial transmission lines, the DAs can achieve a broadband operation, which can theoretically extend from the zero frequency to the cutoff frequency of the artificial line. Despite these advantages, the DAs still encounter several limitations [15], including low gain [16], poor efficiency [17], large chip area [18], and restricted output power [19]. To address these challenges, reactive matching power amplifiers have been proposed, albeit at the expense of increased design complexity.

In this paper, we propose a novel two-stage GaN PA based on the quasi-MMICs and the analysis, design, and implementation for it with a reactive matching network are presented. The high-pass and low-pass filter matching techniques are employed to achieve effective impedance transformation. Resistors are incorporated into the input-stage matching network to improve the circuit stability and enhance gain flatness across the operating band. Based on the proposed design methodology, the amplifier can operate over the frequency range of 2–6 GHz and deliver an output power (P_{out}) of exceeding 60 W with a PAE ranging from 27% to 40% and an averaged small-signal gain of 26 dB. Simulation and experimental results demonstrate the excellent performance of the proposed PA through a comparison with other PAs available in literature.

II. TRANSISTOR MODELING METHODOLOGY

Transistor modeling is a crucial step in amplifier circuit design optimization, and building accurate transistor

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models plays a vital role in optimizing circuit performance [20]. There are two transistor modeling methods: linear small-signal [21] and nonlinear large-signal modeling [22]. Linear small-signal modeling extracts linear parameters through the *S*-parameters in each bias state to establish small-signal models. Large-signal modeling extracts nonlinear parameters based on current-voltage (I-V) test data to establish a large-signal model. By integrating and optimizing the extracted linear and nonlinear parameters, a complete model of the transistor that satisfies both S parameters and IV characteristics is established.

The transistor used in this paper is a GaN high electron mobility transistor (HEMT), which is modeled as a small-signal equivalent circuit using the 15 elements field-effect transistor model, with the structure shown in Fig. 1.

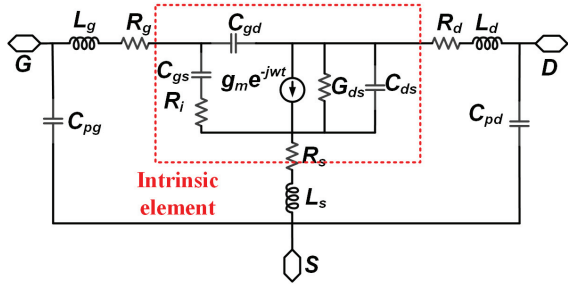


Fig. 1. Small-signal equivalent circuit model.

The parasitic capacitance C_{pg} and C_{pd} are extracted by the Dambrine method [23], the parasitic resistance R_s is extracted by the Yang-Long method [24], and the rest of the parasitic parameters are extracted by the ColdFET method [25]. After extracting the parasitic component parameters, the *S*-parameters can be converted to *Z*-parameters, and the influence of parasitic components can be removed from the *Z*-parameters, i.e., "de-embedding" [26], and the de-embedded *Z*-parameters can be converted to *Y*-parameters to extract the corresponding parameter values of the intrinsic components. The corresponding equivalent circuits of the intrinsic components are shown in Fig. 2.

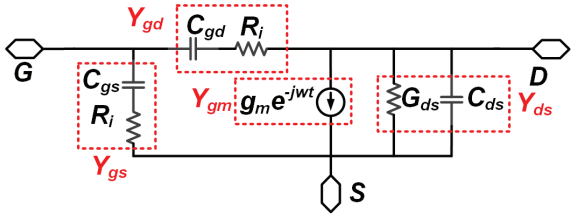


Fig. 2. Intrinsic components equivalent circuit.

While the small-signal model is effective for simulating the linear behavior of the device, accurate prediction of nonlinear characteristics, including DC performance and output power behavior, necessitates the use of a large-signal model. The large-signal model of the traditional HEMT is shown in Fig. 3, in which I_{ds} ("IDS" in Fig. 4), C_{ds}, and C_{gd} are three important nonlinear parameters, each of which has a corresponding nonlinear equation.

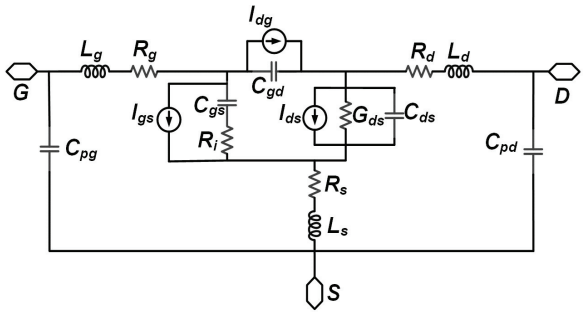


Fig. 3. Conventional HEMT large-signal model.

III. AMPLIFIER ARCHITECTURE

Based on the proposed transistor model, a DC bias scan is applied to the transistor and the results are shown in Fig. 4. Considering the output power and efficiency, the base bias voltage is selected to be −2.4 V and the emitter stage bias voltage is 28 V. At the given bias voltages, the transistor operates in the A and B bias states.

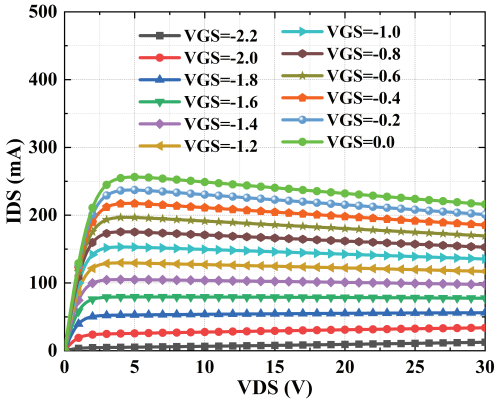


Fig. 4. Load-pull results for the model at 4 GHz.

The core is an eight-cell transistor with a single cell which has the gate width $10 \times 150\ \mu m^2$, transistor capacitance density of 0.45 pF/mm, single cell transistor resistance of 80 Ω, the structure shown in Fig. 5. After extracting the impedance parameters of the power tube core model, the output matching circuit design, if the eight cells are matched separately and then combined to

the RF output and input ports, the branch will become more, increasing the path loss, and the circuit size is too large. To ensure the simplicity and feasibility of the circuit structure design, in the output matching circuit, the eight cells are divided into two four-cell cores, and then the combined design. In the input matching circuit, the octet is divided into four two-cell cores and then combined.

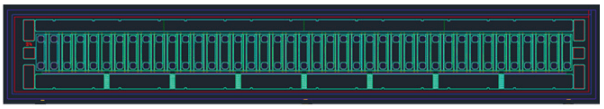


Fig. 5. Octal transistor core.

For the passive components in this circuit, the isolation capacitor and the bypass capacitor adopt the general-purpose non-remaining edge type microwave chip capacitor of Tianji Company, whose upper and lower surfaces are gold electrodes, and the middle ceramic dielectric layer is suitable for the bonding and mounting of gold wires and ribbons, and the structure is shown in Fig. 6. A microwave chip capacitor is a single-layer parallel plate capacitor structure, the capacitance depends on the dielectric constant of the dielectric material (K), the thickness of the dielectric material (T) and the size of the electrode $L \times W$.

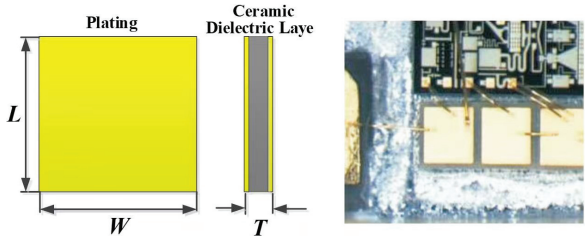


Fig. 6. Schematic and physical drawings of general-purpose no-edge-type microwave chip capacitors.

The designed quasi-monolithic PA consists of a tube core, an output matching circuit and an input matching circuit, and the tube core is connected to the matching circuit by a bonding alloy wire. The length of a single gold wire is 500 μm and the diameter is 25 μm. To realize the high power performance of the amplifier, the output matching circuit is made of alumina substrate, with the dielectric constant of 9.6, thickness of 380 μm, and copper thickness of 35 μm. The input matching circuit is made of a GaAs integrated circuit, with the dielectric constant of 12.9, board thickness of 100 μm, and metal layer thickness of 3 μm.The input matching circuit, the core and the output matching circuit are connected in cascade to obtain the overall structure of the amplifier, which is shown in Fig. 7.

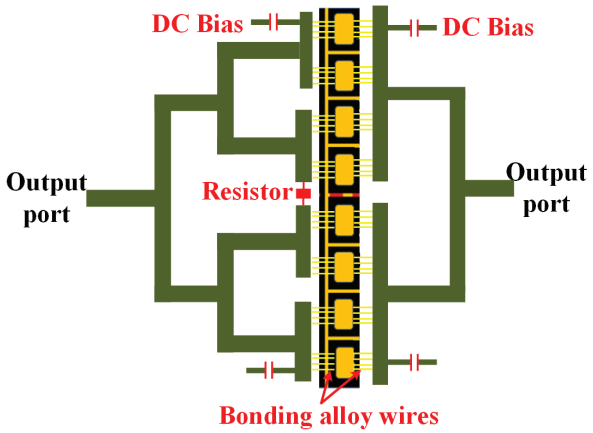


Fig. 7. Schematic diagram of quasi-monolithic amplifier structure.

IV. OVERALL CIRCUIT DESIGN APPROACH

A. Output matching circuit

In power amplifiers, output matching circuits are used to match the optimum output impedance obtained from the transistor by load traction to 50 ohms for maximum output power. The matching circuit is usually realized by using passive devices such as capacitors and inductors as well as microstrip lines, and L-type and ϕ-type structures are commonly used for the structure. When designing the output matching circuit, the octal cell is divided into two four-cell cores, and then the combined design is carried out, the structure is shown in Fig. 8.

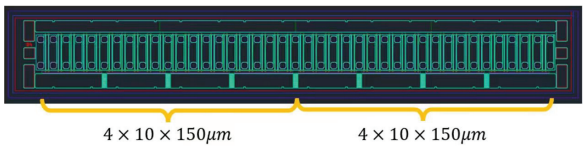


Fig. 8. Schematic diagram of an eight-cell transistor core divided into two equal paths.

The parallel equivalent resistance of a single four-cell core is $80/4 = 20\ \Omega$, and the parallel equivalent capacitance is 0.45 pF/mm$\times$10$\times$150μm$\times$4=2.7 pF. The transistor cores are bonded to the output matching circuit by a total of 36 gold wires, and each 4-cell core is connected in parallel using 18 gold wires, with a total of 36, spaced 130 μm single wires measuring 500 μm in diameter length and 25 μm in diameter. The inductance of a single gold wire is about 1.4 nF.

The constructed output circuit structure is shown in Fig. 9, and it can be seen that the output matching circuit consists of the parallel RC structure corresponding to the core impedance, the imaginary part compensation

network constructed by the bonding alloy wire and the bias feed circuit, the two-order L-type impedance transformation network, and the two-path power synthesis network. Among them, R_o and C_o are equivalent to the optimal output impedance of the four-cell core, L_a is the equivalent inductance introduced by the bonding alloy filament, and the parallel inductor L_b is used to offset the capacitance of the imaginary part of the core impedance, C_o and, at the same time, it plays the role of the drain bias supply. To improve the matching bandwidth, a two-stage low-pass L-type impedance conversion network is used, and the microstrip lines TL1 and TL2 play the roles of impedance conversion and power synthesis.

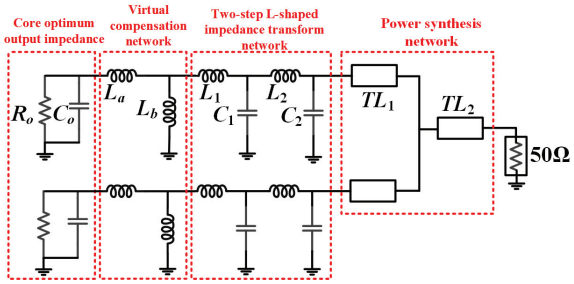


Fig. 9. Output matching network circuit.

Based on the above circuit diagram, an output circuit layout is constructed where the inductors L_b, L_1, and L_2 are in series microstrip line equivalents and the capacitors C_1 and C_2 are in parallel open microstrip line equivalents. A ceramic with a dielectric constant of 9.6 and thickness of 380 μm is used as the substrate for the output matching circuit, and the dimensions of each microstrip line are shown in Table 1. To accurately process the prepared samples, the high frequency structure simulator (HFSS) is used for modeling and simulation regarding the above simulation layout configuration and data based on the advanced design system (ADS). The HFSS model of the output circuit is shown in Fig. 10. The overall size of the structure is about 7.6×11.6 mm^2, and the widths of the microstrip lines are all greater than 100 μm, which can satisfy the maximum current and will not be fused due to overheating.

Table 1: Dimensions of microstrip lines in the output matching circuit

Microstrip Line	Dimension (μm)	Microstrip Line	Dimension (μm)
TL_1	350×1200	TL_2	900×1000
TL_3	2050×3700	TL_4	800×1700
TL_5	700×1000	TL_6	400×700
TL_7	700×1400	TL_8	1200×2000

The overall simulation results of the output matching circuit are shown in Fig. 11, which shows that the

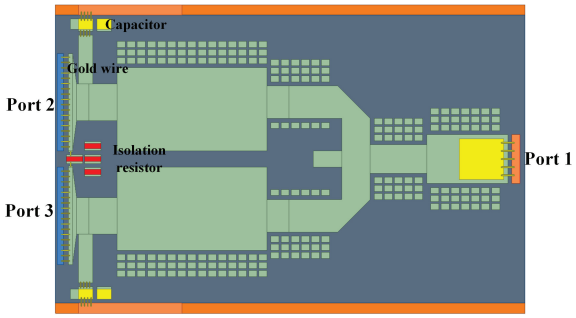


Fig. 10. HFSS modeling of output circuits.

RF output S_{11} is better than -10 dB in the band from 2 to 6.22 GHz, the drain output S_{22} is better than -7 dB in the band from 2 to 6 GHz, and the insertion loss S_{21} is better than -3.8 dB in the band range from 2 to 6.2 GHz. Taking into account that the actual loss conditions will produce a frequency-shift phenomenon, it would be better to extend the extended to about 6.2 GHz at high frequencies.

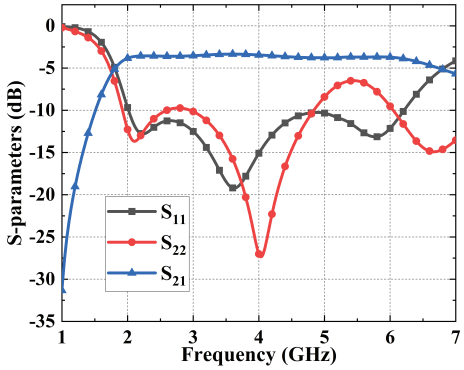


Fig. 11. Simulation result of S parameters for the output matching circuit.

B. Input matching circuit

In terms of the input matching circuit, the matching circuit is constructed by equalizing four two-cell merge circuits for the tube core, and the structure is shown in Fig. 12. The input circuit is realized using a 0.35 μm GaAs monolithic process to equalize the input signal into four two-cell transistor ports, with the output impedance of each circuit set to 40 Ω, and the output impedance of the four parallel combined circuits is 10 Ω.

The input matching circuit construction method is similar to the output matching circuit, in order to ensure a wide bandwidth of low insertion loss and the overall gain of the amplifier within the bandwidth, the use of type microstrip line structure, loading capacitors and other passive components to build matching network,

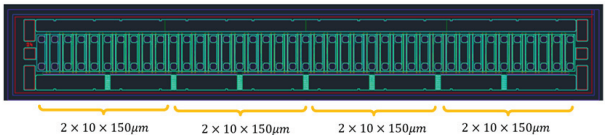


Fig. 12. Schematic diagram of an eight-cell transistor core divided into four equal paths.

the circuit is shown in Fig. 13. It can be seen that the input matching circuit consists of a series RC structure corresponding to the impedance of the core, the imaginary part of the compensation network constructed by the bonding alloy wire and the bias feed circuit, the third-order L-type impedance transformation network and the power synthesis network. Among them, R_o and C_o are equivalent to the input impedance of the double-cell core, L_a is the equivalent inductance introduced by the bonding alloy wire, and the parallel inductance L_b plays the role of gate bias power supply while it is used to offset the imaginary part of the core impedance capacitance C_o. To improve the matching bandwidth, a three-stage low-pass impedance conversion network is used, and the microstrip lines TL1 and TL2 play the role of impedance conversion and power synthesis at the same time.

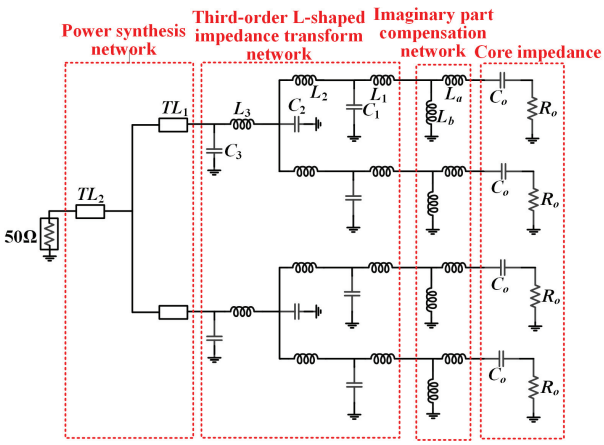


Fig. 13. Input matching circuit structure.

The structure of the input matching circuit is shown in Fig. 14, and the dimensions of each microstrip line are shown in Table 2.

The above input matching, tube core and output matching modules are cascaded to construct the overall circuit structure of the amplifier, and the circuit structure is shown in Fig. 15. Based on the transistor small-signal model and the S-parameters extracted from the output matching circuit, the S-small-signal simulation circuit of the amplifier is constructed. The impedance of input port 1 is 50 Ω. The small-signal simulation results of the

Table 2: Dimensions of microstrip lines in the input matching circuit

Microstrip Line	Dimension (μm)	Microstrip Line	Dimension (μm)
TL_1	806×67	TL_2	135×50
TL_3	820×50	TL_4	1790×50
TL_5	870×50	TL_6	260×50
TL_7	548×50	TL_8	1286×2000
TL_9	289×50	TL_{10}	463×50
TL_{11}	602×65	TL_{12}	202×65
TL_{13}	347×65	TL_{14}	187×65
TL_{15}	582×65	TL_{16}	141×65
TL_{17}	300×100	TL_{18}	1000×100
TL_{19}	1000×100		

amplifier are shown in Fig. 16, and the output port S_{22} is better than -12 dB in the range of $2-6$ GHz, the input S_{11} is better than about -5.6 dB in the band range of $2-6$ GHz, and the gain S_{12} is better than 10 dB in the range of $2-6$ GHz.

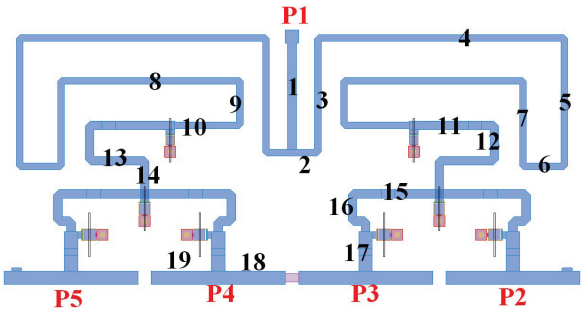


Fig. 14. Structure and layout of input matching circuit.

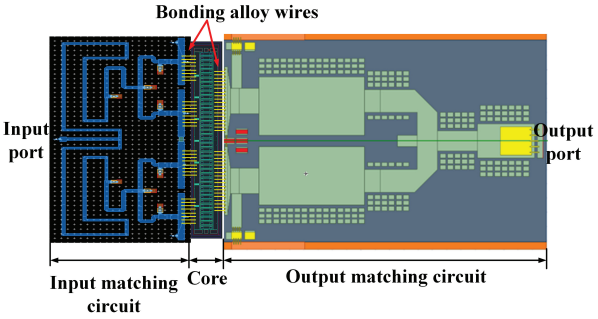


Fig. 15. Circuit structure of the $2-6$ GHz quasi-monolithic amplifier.

V. AMPLIFIER CIRCUIT SIMULATION AND TEST RESULTS

Based on the above amplifier structure, a physical sample is prepared as shown in Figs. 17 and 18, in which

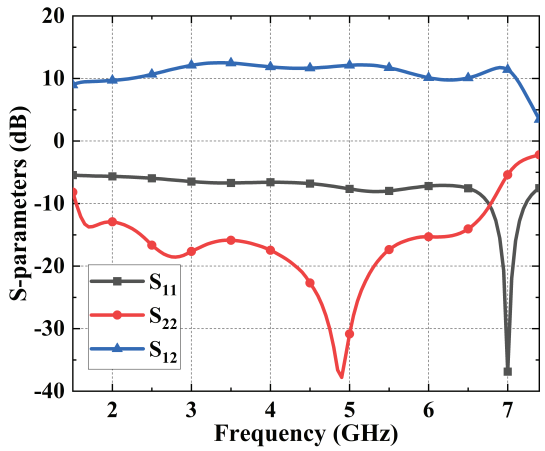


Fig. 16. Simulation results of S_{11}, S_{22}, and S_{12} parameters with a small-signal for the $2-6$ GHz quasi-monolithic amplifier.

the bias voltage is set to -2 V and 28 V. The amplifier is subjected to small-signal testing of S-parameters, gain, and other small-signal performances in the range of $2-6$ GHz, and the small-signal performances are obtained by on-chip testing using a vector network analyzer and so on. The small-signal test and simulation results of the amplifier are shown in Fig. 19, and the measured results show that the amplifier fluctuates between $12-15$ dB in the $2-6$ GHz range.

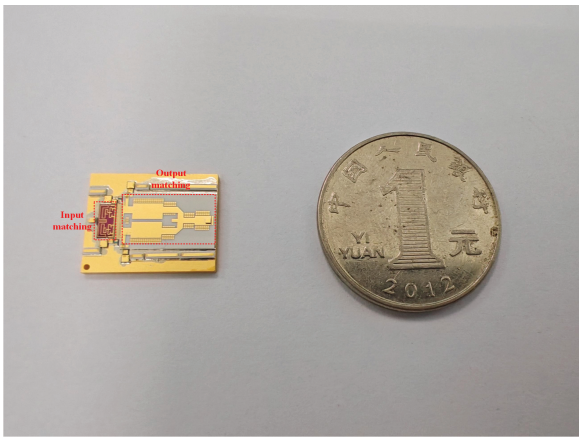


Fig. 17. A sample of matching circuit.

The large-signal test of the amplifier is conducted to measure the output power and saturated power added efficiency of the amplifier at the $2-6$ GHz band. The block diagram of the large-signal test connection and the test results are shown in Fig. 20. From the test results, it can be seen that the saturated output power of the amplifier is in the range of $48-50$ dBm in the $2-6$ GHz range, and the gain additive efficiency PAE is $34\sim46\%$.

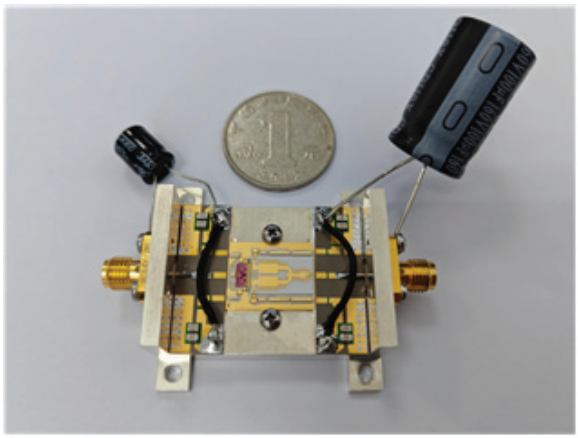


Fig. 18. A sample of the $2-6$ GHz quasi-monolithic amplifier.

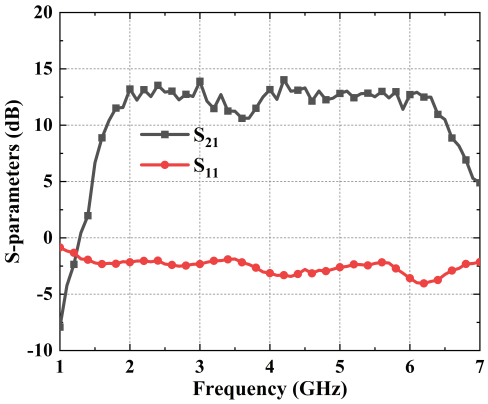
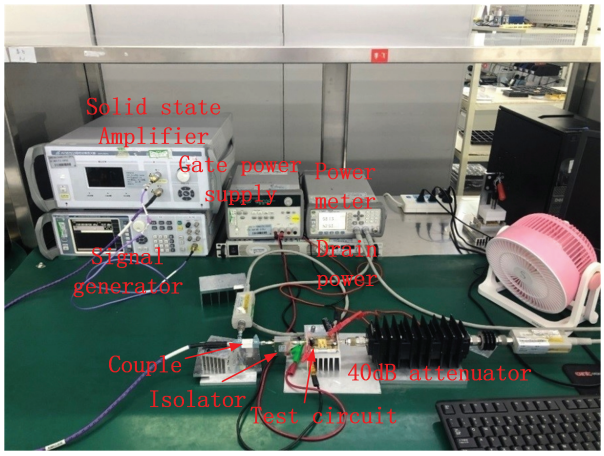


Fig. 19. Simulation results of S_{21} and S_{11} parameters with a small-signal for the $2-6$ GHz quasi-monolithic amplifier.

The performances of this PA is compared with other quasi-monolithic microwave integrated circuit (MMIC) ultra-wideband GaN PAs available in literature [21–26] and the result is shown in Table 3. The proposed PA can achieve an excellent performance with a bandwidth of $2.0\sim6.0$ GHz, a gain of 11.0 dB, a saturated output power (P_{sat}) of 48.0 dBm, and a maximum PAE of 34.0%. Compared with the performance indexes of those PAs from the references, the proposed PA has the highest value of figure of merit (FoM) which is defined by $FoM_{PA} = P_{sat} + 10\log[PAE_{max}(\%)] + Gain + 10\log[BW_{3dB}/f_0]$, where f_0 is the central frequency of the frequency band.

For the thermal effect of the amplifier, we have conducted a test and the results are shown in Fig. 21. From Fig. 21, we can see that the heat of the amplifier mainly concentrates in the input matching circuit and the maximum temperature is 106°.



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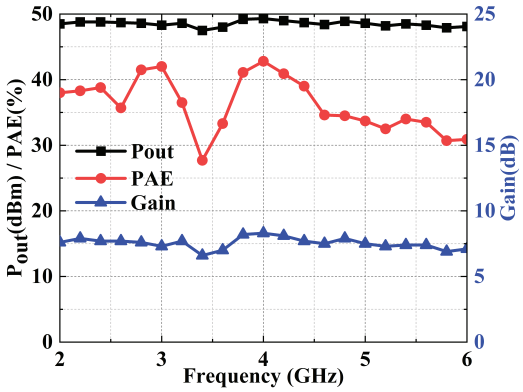

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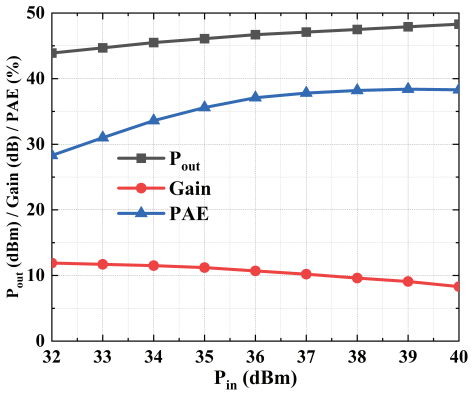

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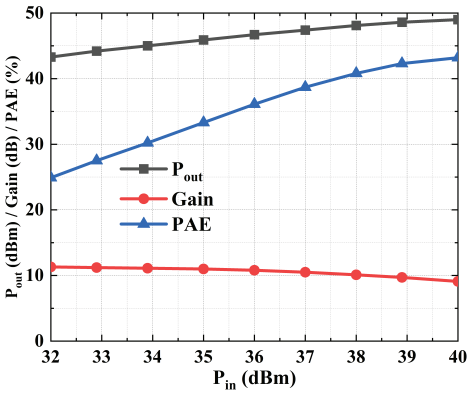

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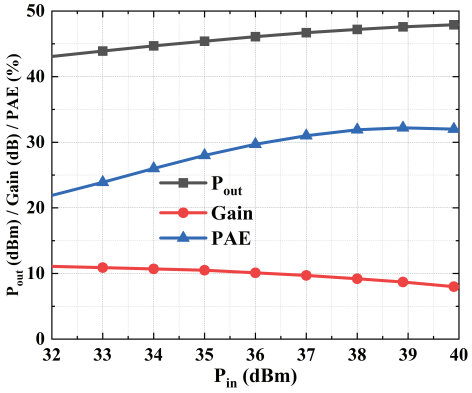

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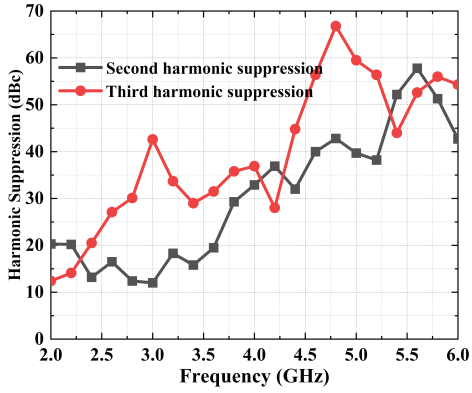

(f)

Fig. 20. Test results for the performance of the proposed PA. (a) Test setup. (b) Changes of P_{out}, gain, and PAE as a function of frequency. (c) Changes of P_{out}, gain, and PAE in terms of P_{in} at 2.0 GHz. (d) Changes of P_{out}, gain, and PAE in terms of P_{in} at 4.0 GHz. (e) Changes of P_{out}, gain, and PAE in terms of P_{in} at 6.0 GHz. (f) Suppression effect of harmonic waves.

Table 3: Performance summary and comparison of different distributed amplifiers

Reference	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	PAE$_{max}$ (%)	Bandwidth (%)	FoM	Technology
[27]	1.8-3.2	9.0	41.4	36.0	56.0	83.4	250-nm GaN
[28]	8.4-9.8	7.4	50.4	36.0	15.4	85.2	250-nm GaN
[29]	1.0-1.6	10.5	47.0	27.0	46.0	88.4	GaN HEMT
[30]	5.5-6.5	12.5	44.0	40.0	16.7	84.7	250-nm GaN
[31]	8.4-8.6	5.0	35.0	45.0	2.3	60.1	GaN HEMT
[32]	2.0-4.0	9.8	46.5	38.0	33.3	87.3	500-nm GaN
This Work	2.0-6.0	11.0	48.0	34.0	100.0	94.3	350-nm GaN

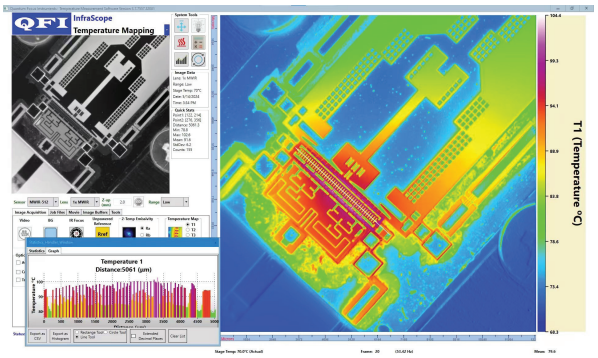

Fig. 21. Test result of thermal distribution for the 2-6 GHz quasi-monolithic amplifier.

VI. CONCLUSION

In this paper, a $2-6$ GHz broadband quasi-monolithic amplifier design method is proposed, with the GaN HEMT structure for the tube core, GaAs monolithic microwave integrated circuits for the input matching circuit of the amplifier, and high dielectric constant ceramic substrate for the output matching circuit. The core is a single-cell size gate width of the eight-cell transistor, the output matching circuit will be divided into eight-cell equal to two four-cell core, the input matching circuit will be divided into eight-cell equal to four two-cell core, through the multi-order L-type impedance transformation structure to achieve impedance matching after the design of the combined circuit. The test results show that the amplifier saturates the output power P_{out} in the range of $2.0-6.0$ GHz band at $48-50$ dBm, and the gain added efficiency PAE is $34-46\%$.

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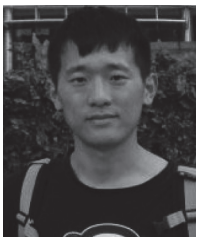

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