GPU Based TLM Algorithms in CUDA and OpenCL

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***Abstract*—** Recent advancements in graphics computing technology has brought highly parallel processing power to desktop computers. As multi-core multi-processor computing technology becomes mature, a new front in parallel computing technology based on graphics processing units has emerged. This paper reports a highly parallel symmetrical condensed node TLM procedure for the NVIDIA graphics processing units. The algorithm has been tested on three NVIDIA processors, from low-end laptop graphics card to high-end workstation graphics processors.

***Index Terms*—** TLM, FDTD, GPU, SIMD, time-domain, parallel computing, stream computing.

I. INTRODUCTION

Graphics processing unit (GPU) based parallel computing has been an important topic for the computing industry for over a decade. Macedonia addressed this topic in a computing magazine article in 2003 [1]. Most of the papers on GPU computing were related to signal and image processing [2–6]. Krakiwsky *et al.* and Inman *et al*. applied the technique to accelerate the FDTD algorithm [7, 8]. Takizawa *et al.* applied GPU computing to heat transfer simulation [9]. Z. Luo *et al.* and Harding *et al.* applied the paradigm to artificial neural network [10] and genetic algorithm [11], respectively. Furthermore, a cluster of GPU based computers can be created to execute grand challenge problems [12]. Researchers at Stanford [13] have been using this technique for years in protein folding computation.

Developing general purpose numerical modules for GPU was made easy by NVIDIA. The company released its Compute Unified Device Architecture (CUDA) Software Development Kit (SDK) in early 2007. The SDK enables programmers to develop GPU code in a high level language, *C-for-CUDA*. Rossi *et al*. reported the first implementations of a two- and a three-dimensional transmission line matrix (TLM) [14-17] program using the CUDA SDK [18]. This highly parallel TLM code has been ported to the new released OpenCL [19] environment. This makes it possible to run the program on non-NVIDIA GPUs and on heterogeneous computing hardware (for instance, GPU based computers with multiple multi-core CPUs). This paper addresses the algorithm design, programming techniques, and performance issues for implementing GPU based programs; in particular, the pros and cons of choosing CUDA and OpenCL will be discussed.

II. GPU COMPUTING

Modern GPU designs architectures are based on the Single Instruction Multiple Data (SIMD) computing paradigm. This hardware architecture utilizes multiple processors to perform similar tasks on vast quantities of data. The appeal for GPUs exists not only because of their computational ability, but also given that they are relatively inexpensive and can be installed on existing workstations. The NVIDIA GPUs used in this project are GeForce 8800 Ultra, Quadro FX 570M and Quadro FX5600 graphics cards [20]; these GPUs have 4 to 16 multi-processors with 8 processors each for a total of 32 to 128 processors. The GPUs have a maximum of 1.5 GB of GDDR3 global memory. A schematic that depicts the computing model of the NVIDIA GPU using a layer of a TLM mesh is shown in Fig. 1. The figure illustrates a typical iteration cycle. The data structure to be processed (called a mesh) is defined in both the CPU and the GPU. After seeding a data structure with initial conditions, the host transfers the data to the GPU's global memory and constant memory. A GPU function (called a kernel) would then be invoked which would execute on all multi-processors (4 to 16). This computing paradigm is scalable by utilizing GPU clusters internal or even external to a workstation [21]. Adaptation to GPUs is suitable for many science and engineering applications. However, the parallelization of existing algorithms may require intricate and complex adaption efforts.

The driving forces behind the computing framework depicted in Fig. 1 are the thread-blocks that control the GPU executions, Fig. 2. A thread block is defined as a grouping of threads that executes concurrently on the GPU multi-processors. Multiple data elements could be

assigned per thread (data block). A maximum of 512 threads per thread block are available for the GPUs, therefore it is then necessary to partition the mesh into data blocks. Each multi-processor would, in turn, execute on a data block utilizing its thread-block and then transfer the results back to the global memory. After which the multiprocessor would download the next available data block. The 16 multi-processors on the graphics card used in this project worked concurrently and are coordinated to process all data blocks in the global memory.

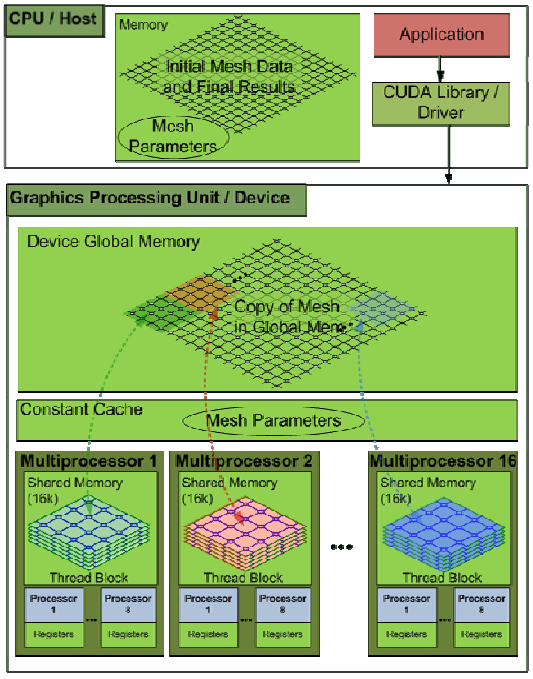


Fig. 1. NVIDIA CUDA based GPU computing framework.

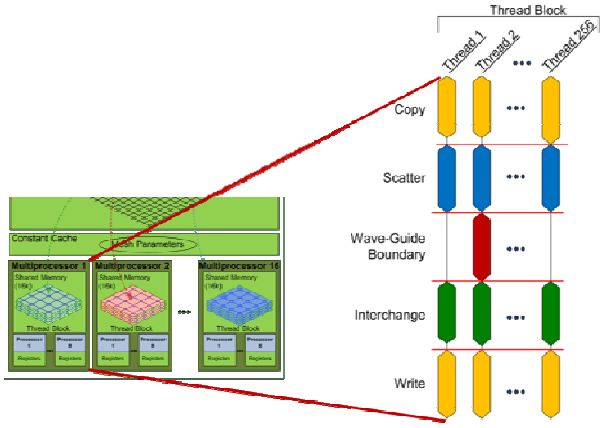
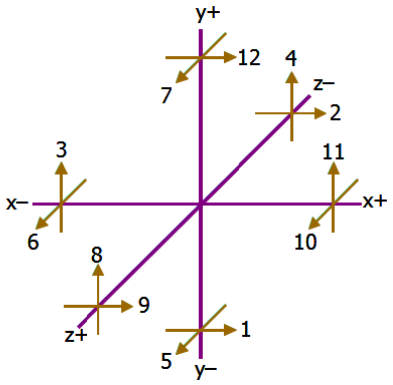


Fig. 2. NVIDIA CUDA based GPU computing framework.

III. SYMMETRIC CONDENSED NODE TLM

The three-dimensional symmetrical condensed node (SCN) is depicted in Fig. 3. The fundamental procedures in a TLM algorithm are the scattering, transfer and reflection of voltage impulses, [17]. There are two orthogonal transmission link lines in each port of the TLM node. Voltage impulses travelling along the *x*-axis are polarized in the *y*- or *z*-direction; similarly voltage impulses on the *y*- and *z*-axis are polarized in the other two orthogonal directions on the plane transverse to the direction of propagation. Hence, there are a total of 12 voltage impulses in each symmetrical condensed node. The scattering matrix for the symmetrical condensed node TLM method is a 12×12 matrix [17]. Therefore, a matrix multiplication operation can be used to obtain the reflected voltage vector from the incident voltage vector. The other two TLM operations are transfer of impulses to the neighboring link lines and reflection of impulses at material boundaries, Fig. 4. These two operations are applied to the two orthogonally polarized voltage impulses. All three TLM operations — scattering, transfer and reflection of voltage impulses — are localized operations which may be executed in parallel to reduce computing time. A quad-core processor may execute each operation concurrently for four TLM



$$[V]_{k+1}^{r} = [S] \times [V]_{k}^{i}$$

$$[S] = \begin{bmatrix}
a & a & & & & & a & -a & & & & \\
a & & & & a & & & -a & a & & & \\
a & & a & & & a & & & -a & & & \\
 & a & & a & & -a & & & & a & & \\
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\end{bmatrix}$$

Fig. 3. SCN scattering algorithm.

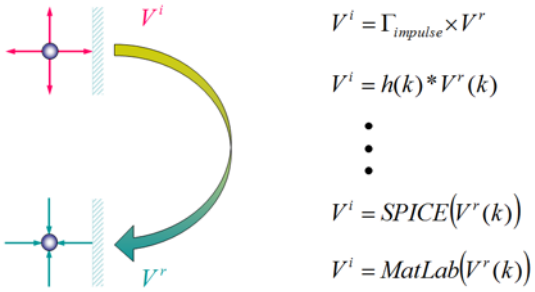

Fig. 4. TLM boundary operation.

nodes. A traditional serial TLM program can be easily parallelized by using OpenMP [22] compiler directives. However, the number of cores on a single CPU is small and the gain in performance by using OpenMP is therefore still limited. With GPUs, numerical procedures such those described above can be executed in parallel on a much larger scale.

IV. IMPLEMENTATION

Efficient use of multiprocessor resources, especially global memory transfer strategies, can help to achieve close to the maximum theoretical operating speeds of GPUs. Memory transfer rates between the global memory and multiprocessors can be used as a benchmark for GPU performance since much of the kernel execution time (70% to 80%) may be spent in accessing global memory. In the case of the Quadro FX 5600, the maximum theoretical memory bandwidth to global memory is 76.8 GB/sec [21] or expressed as read+write round trip: 38.4 GB/sec.

Memory coalescing is a performance enhancement technique whereby access to global memory by multiprocessors can be accelerated [20]. Global memory (GDDR3 memory) consists of physical banks of memory. Access to global memory by any of the multiprocessors results in 400-600 clock cycles of latency. In other words, each four byte float or integer copied from or written to global memory takes 400-600 clock cycles. Since the GDDR3 global memory exists physically as banks of memory, reads/writes can be organized such that [20]:

1. The starting address of each half-warp (16 threads) falls on a 64 byte interval
2. Each thread of a half-warp reads/writes 4, 8 or 16 bytes consecutively
3. The threads of each half-warp must be spaced at 4, 8 or 16 byte intervals.

Figure 5 illustrates the differences in memory access speed (GB/sec read-write round trip) between coalesced code (~25 GB/sec) and non-coalesced code (~3 GB/sec). A speed-up of over 8 times for coalesced kernel code warranted developing TLM kernel that adhered to coalescing coding strategies.

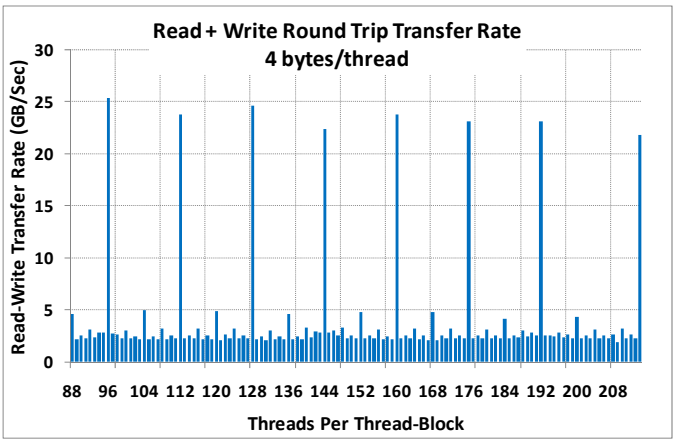

Fig. 5. GPU performance differences between coalesced a non-coalesced memory configurations.

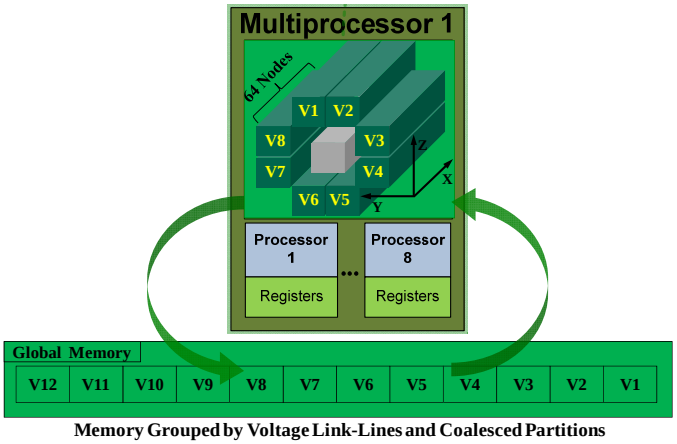

Fig. 6. Coalesced global memory access by thread-blocks of multiprocessors.

The TLM kernel is designed such that global memory is grouped by voltage link lines (12 per TLM node), and accessed by the multiprocessors in a coalesced manner to take maximum advantage of the GPUs speed performance, Fig. 6. The resolution of the Y and Z dimensions of a mesh is each one node wide. However, the X dimension is partitioned into 64 node segments. The addressing is thus contiguous, first in the x-direction, then the y-direction and finally the z-direction. The thread-block dimension is defined at 64 threads, where the kernel would read a voltage link line for 64 nodes at a time in the x-direction. For example, 64 values of V1 would be read for 64 nodes, then for V2 would be read for the same 64 nodes and so on until all 12 voltagess have been read so that the scattering

procedure may commence on 64 nodes. Writing results back to global memory is done in a similar manner. Fig 7 showcases the performance enhancement of configuring the TLM kernel in a coalesced fashion.

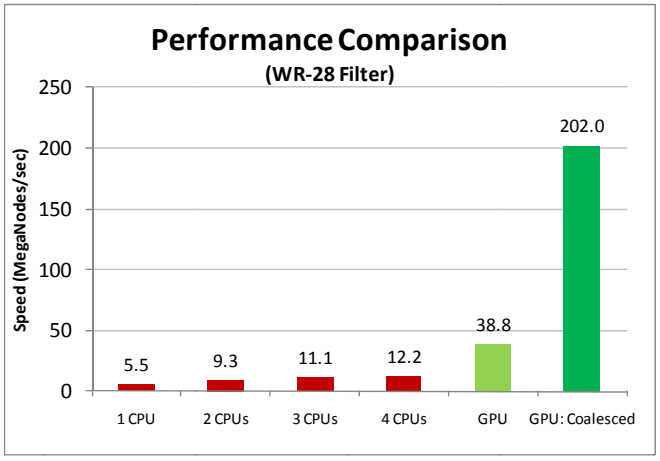

Fig. 7. TLM codes performance on 1 to 4 CPUs. The codes were used to analyze a WR-28 filter (150,000 nodes). The GPU codes have a non-coalesced GPU kernel and a coalesced GPU Kernel.

V. OPENCL IMPLEMENTATION

The newly released OpenCL application programming interface (API) has many features found in the CUDA paradigm. In fact, once a program has been developed using the CUDA framework, it is not difficult to implement an equivalent version in OpenCL. This is especially true if the NVIDIA's "Driver API" method is used instead of "C for CUDA" [19]. Both OpenCL and the Driver API standards are handle-based hence objects to memory and functions are required. However, OpenCL differs in its ability to utilize a heterogeneous mixture of parallel hardware. An OpenCL application can utilize a mixture of GPUs, CPUs, and other processors. Therefore OpenCL is a powerful API for integrating multiple parallel platforms under one cohesive programming paradigm.

Figure 8 depicts some equivalent programming constructs in the two APIs. As shown in the figure most of the equivalent constructs have meaningful mapping from CUDA to OpenCL; the only exception in the table is the "Local Memory" construct.

In addition to systemically replacing the programming constructs, it is also necessary to substitute CUDA kernel code attribute modifiers with equivalent OpenCL methods, Fig. 9. A short code segment that illustrates the code transformation concept is shown in Fig. 10. When compared to CUDA, OpenCL is a relatively new API hence it is less efficient than CUDA especially when the problem size is small. Figure 11 compares the performance of our CUDA and OpenCL TLM code. When the structure size reaches about 10 million nodes, the two programs have similar computation speed.

CUDA	OpenCL
Thread	Work-item
Thread Block	Work Group
Shared Memory	Local Memory
Local Memory	Private Memory

Fig. 8. Equivalent programming constructs in CUDA and OpenCL.

CUDA Kernel Code	OpenCL Kernel Code Replacement
gridDim	**get_num_groups(*n*)**
blockDim	**get_local_size(*n*)**
blockIdx	**get_group_id(*n*)**
threadIdx	**get_local_id(*n*)**
__global__ function (callable from host, not callable from device)	**__kernel** function (callable from host or device)
__device__ function (not callable from host)	
__constant__ variable declaration	**__constant** variable declaration
__device__ variable declaration	**__global** variable declaration
__shared__ variable declaration	**__local** variable declaration
__syncthreads()	**barrier()**

Fig. 9. Attribute transformation table.

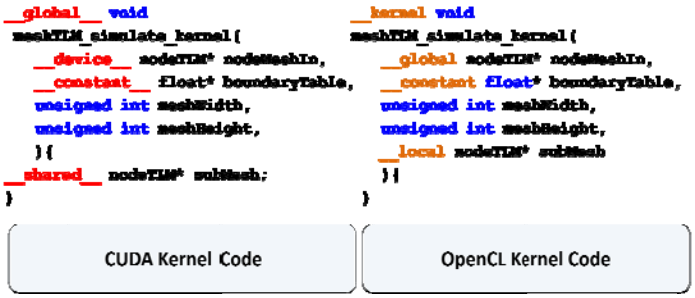

Fig. 10. Kernel code transformation.

VI. CONCLUSION

We have successfully designed and implemented a highly parallel SCN TLM algorithm for the CUDA/OpenCL enabled NVIDIA GPU. It is found that both CUDA and OpenCL are good programming APIs for implementing computational intensive applications such as TLM on GPU based hardware. Our latest CUDA implementation of the 3D SCN TLM routine has achieved a 293 MNodes/sec performance of an empty

structure and 288 MNodes/sec with the filter implemented. Ongoing research activities are focusing on improving the speed of execution and adapting the

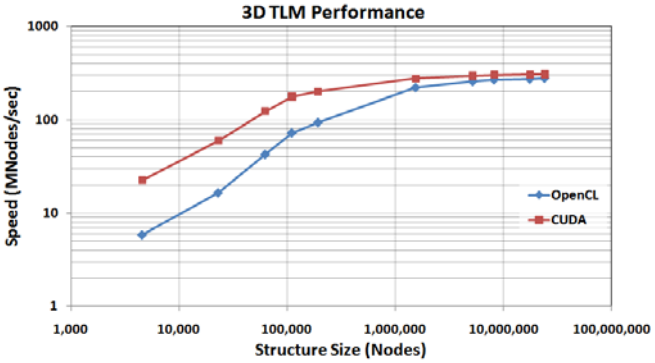

Fig. 11. Performance comparison — CUDA versus OpenCL.

algorithms to solve various structures and configurations. An investigation in utilizing a cluster of 4 NVIDIA GPUs on an Acceleware ClusterInABox™ Quad Q30 workstation is being conducted. The implementations described above can be modified to handle the generalized symmetrical condensed node (GSCN) TLM algorithm developed by Trenkic *et al.* [23, 24]. The total number of voltage impulses to be stored per node would thus increases from 12 to 18. This would reduce the number of nodes each multi-processor thread-block can handle. However the GSCN scattering procedure would not cause any significant reduction on the overall performance as the bottleneck is in the data transfer, not in number of floating point operations. Hence, the performance results depicted in figures 8 and 12 are still valid but the code would reach the maximum acceleration at a smaller structure size.

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