Performance of Single and Double T-matched Short Dipole Tag Antennas for UHF RFID Systems

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Abstract ─ The impact of tag antenna and chip impedance tolerances on power transfer between these components is investigated analytically. Means for efficient computation of the minimum and maximum power transmission coefficient under given impedance tolerances are developed. The presented sensitivity analysis is employed to quantify the design uncertainty of single and double T-matched short dipole tag antennas for UHF RFID systems. The simulated and measured performance of the two tag antennas is analyzed and compared.

IndexTerms ─ Double T-matching, impedance matching, passive UHF RFID, tag antenna, T-matching.

I. INTRODUCTION

In radio-frequency identification (RFID) systems, electromagnetic interaction between a reader and electronic labels, designated as RFID tags, is employed to identify objects. In ultra high frequency (UHF) RFID systems, the mechanism of the interaction is most commonly wave propagation and the RFID tags are antennas loaded with a microchip. Passive RFID tags, which are studied in this article, scavenge energy for their operation from the incident electromagnetic field sent by the reader. In addition to capturing energy with on-chip rectification, the chip stores a unique electronic product code to label the tagged object, demodulates commands from the reader and creates a response to the reader's queries. Tag's response is created by switching the chip impedance between two values while the reader illuminates the tag with a single-frequency electromagnetic field. As a result, the tag's response is modulated in the load-dependent component of the electromagnetic field scattered from the tag antenna [1].

As the passive RFID tags are not equipped with an energy source, maximizing the power delivery from the tag antenna to the chip is often the principal goal in tag design. However, the boundary conditions for the design are stringent. For a globally operable UHF RFID tag, good antenna performance is required over a broad, 10% fractional bandwidth (from 860 MHz to 960 MHz), while compact and low-profile antenna structures are preferred for seamless integration with objects. Thus, small antenna features are a crucial tag antenna design aspect. Furthermore, the unit cost of the tag antenna needs to be minimal when labelling a large asset base with RFID tags. To achieve cost-savings in the antenna manufacturing, most commonly the complex conjugate impedance matching between the tag antenna and the chip is arranged by designing the tag antenna geometry so that appropriate antenna impedance is achieved together with the desired radiation characteristics. In this process computational electromagnetics is extensively employed.

Dipole-type tag antennas are popular in UHF RFID systems. They benefit from being structurally simple radiators with omnidirectional radiation pattern, which allows the detection of

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dipole tags from all directions in a plane normal to the tag. Moreover, clever size reduction and impedance matching techniques for them have also been extensively investigated in general context [2-5] as well as for RFID applications [6-8]. This article focuses on RFID tag antenna design verification based on impedance tolerances and on the performance comparison of single and double T-matched short dipole tags.

The rest of the article is organized as follows. Section II introduces the concept of power transmission coefficient and discusses the efficient computation of its limits under given source and load impedance variations. In Section III, the simulation based design of single and a double T-matched short dipole tag antennas is discussed and the prototype antennas as well as simulation results are presented. Section IV focuses on experimental verification of the simulation-based designs and presents the comparison of the simulation and measurement results. Finally, conclusions are drawn in Section V.

II. IMPACT OF IMPEDANCE TOLERANCES ON POWER TRANSFER

Power transfer from the tag antenna to the chip can be analyzed by considering two complex impedances connected with a transmission line with negligible electrical length. In this case, the ratio of the power available from the tag antenna (P_{tag}) and the power reflected back (P_{rfl}) from the antenna-chip interface due to impedance mismatch is given by [10]

$$\frac{P_{rfl}}{P_{tag}} = \left| \frac{Z_{ic} - Z_a^*}{Z_{ic} + Z_a} \right|^2, \tag{1}$$

where $Z_a=R_a+jX_a$ and $Z_{ic}=R_{ic}+jX_{ic}$ are the antenna and chip impedances, respectively and $(\cdot)^*$ denotes complex conjugation. As the delivered power to the chip is the difference $P_{ic}=P_{tag}-P_{rfl}$, using (1), the power transmission coefficient (τ) between the tag antenna and chip is expressed as

$$\tau = \frac{P_{ic}}{P_{tag}} = 1 - \frac{P_{rfl}}{P_{tag}} = \frac{4R_a R_{ic}}{\left| Z_a + Z_{ic} \right|^2}. \tag{2}$$

In practice, neither the tag antenna nor the chip impedance is known exactly and due to the nonlinearity of (2) it is difficult to predict the magnitude of the impact of impedance variations on the power transfers without a more rigorous analysis. Thus, it is of practical interest to evaluate the maximum deviation of τ from its nominal value while assuming the tag antenna and the chip impedances lie in the neighborhood of their nominal values $Z_{a0}=R_{a0}+jX_{a0}$ and $Z_{ic0}=R_{ic0}+jX_{ic0}$, respectively. For the purposes of the presented analysis, these neighbourhoods are defined below as rectangles in the chip and antenna impedance planes.

Let $0<p,r<\infty$, $0<q,s<\infty$, and $0<\varepsilon<\min(p,r)$ and consider sets defined as

$$\begin{aligned} D_\varepsilon &= \left\{ (x,y) \in R^2 : x \geq \varepsilon,\ y \in R \right\}, \\ \Lambda_{pq} &= \Big\{ (x,y) \in R^2 : \left| R_{ic0} - x \right| \leq p R_{ic0}, \\ &\qquad \left| X_{ic0} - y \right| \leq q \left| X_{ic0} \right| \Big\} \bigcap D_\varepsilon, \\ \Lambda_{rs} &= \Big\{ (x,y) \in R^2 : \left| R_{a0} - x \right| \leq r R_{a0}, \\ &\qquad \left| X_{a0} - y \right| \leq s \left| X_{a0} \right| \Big\} \bigcap D_\varepsilon. \end{aligned} \tag{3}$$

Under these definitions, Λ_{pq} and Λ_{rs} are rectangles centered at the nominal chip and tag antenna impedances, respectively, and restricted in the half-plane containing the positive resistances. The size of these rectangles is determined by the parameter pairs (p,q) and (r,s) with r and p defining the percentage tolerance in R_a and R_{ic}, respectively, and the parameters s and q defining the percentage tolerance in X_a and X_{ic}, respectively. In the special case $0<p,r<1$, the set D_ε along with the positive and arbitrarily small number ε could be dropped from the definition (3), as in this case the imaginary axis, where (2) is not necessarily well-defined, is always excluded from the sets Λ_{pq} and Λ_{rs}. However, as discussed in Section III, large values of p and r may be needed in evaluation of platform-tolerance of RFID tags based on the analysis presented in the Section II A. Therefore, p and q are not considered upper bounded, but rather the set D_ε is used to keep (2) well-defined in Λ_{pq}, Λ_{rs}. Moreover, these sets are nonempty and closed by definition. These properties are also required in the presented analysis.

A. Minimum τ under given impedance tolerances

Treating τ first as a function of the chip impedance only, while considering the antenna impedance fixed and calculating the directional derivative of τ along a vector u point from the

perfect conjugate match impedance point $(R_{a0},-X_{a0})$ to an arbitrary point $(R_{ic}, X_{ic})\in D$, one finds

$$D_u\tau = -\frac{4R_{a0}\left(R_{a0}+R_{ic}\right)\left(\left(R_{a0}-R_{ic}\right)^2+\left(X_{a0}+X_{ic}\right)^2\right)}{\left(\left(R_{a0}+R_{ic}\right)^2+\left(X_{a0}+X_{ic}\right)^2\right)^2} < 0,\ \forall\left(R_{ic}, X_{ic}\right)\in D\setminus\left\{\left(R_{a0},-X_{a0}\right)\right\}. \quad (4)$$

This shows that τ is a strictly decreasing function of the chip impedance in D towards directions away from the perfect conjugate match impedance point $(R_{a0},-X_{a0})$, where it attains its maximum value $\tau=1$. Equation (4) also implies the uniqueness of this maximum within D.

Starting from (2), it is shown that the chip impedances corresponding to a constant τ define a circle with center point $P(\tau)$ and radius $r(\tau)$ given by

$$P(\tau)=\left(R_{a0}\frac{2-\tau}{\tau},-X_{a0}\right) \quad \text{and} \quad r(\tau)=2R_{a0}\frac{\sqrt{1-\tau}}{\tau}. \quad (5)$$

This circle always encloses the perfect conjugate match impedance point $(R_{a0},-X_{a0})$, where τ is maximized. Since a rectangle can always be enclosed in a circle touching one of its corners, particularly the rectangle Λ_{pq} defined in equation (3) can always be enclosed in a constant τ circle touching one of its corners.

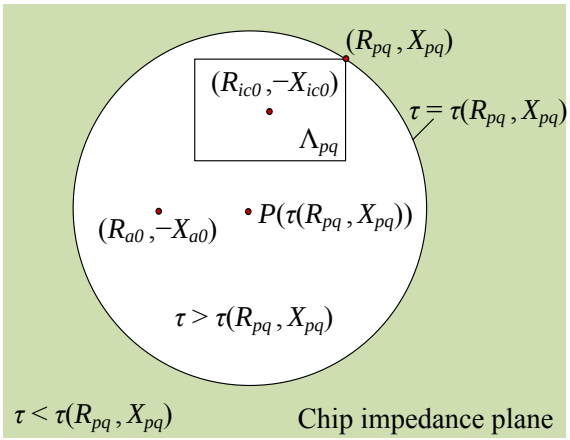


Fig. 1. A constant power transmission coefficient circle enclosing the uncertainty rectangle Λ_{pq} in the chip impedance plane.

To elaborate on the implications of this geometric observation, let (R_{pq},X_{pq}) be the corner discussed above. As the perfect conjugate match impedance point $(R_{a0},-X_{a0})$ is always contained in the circle (5), equation (4) then guarantees that at any point in Λ_{pq}, except for (R_{pq},X_{pq}), it holds $\tau>\tau(R_{pq},X_{pq})$. This means that the minimum value of τ in Λ_{pq} is always attained at a corner of the rectangle Λ_{pq}. This is illustrated in Fig. 1.

As seen from equation (2), the expression of τ is symmetric with respect to pairs (R_a,X_a) and (R_{ic},X_{ic}). Therefore, all the above conclusions of τ as a function of the chip impedance are valid also when τ is treated as a function of the tag antenna impedance, while considering the chip impedance fixed. Consequently, for all $(R_{ic},X_{ic};R_a,X_a)\in\Lambda_{pqrs}=\Lambda_{pq}\times\Lambda_{rs}$, one obtains

$$\begin{aligned}\tau(R_{ic},X_{ic};R_a,X_a) &\geq \tau(R_{pq},X_{pq};R_a,X_a)\\ &\geq \tau(R_{pq},X_{pq};R_{rs},X_{rs}),\\ &= \tau_{min},\end{aligned} \quad (6)$$

where (R_{pq},X_{pq}) is a corner of Λ_{pq} and (R_{rs},X_{rs}) is a corner of Λ_{rs}. Obviously, as the lower bound for τ obtained in (6) is actually the function itself evaluated at a point in Λ_{pqrs}, τ_{min} is necessarily a minimum of τ within this set.

In practice, this value is calculated as the minimum of τ evaluated at the 16 corners of the 4-dimensional rectangle Λ_{pqrs}. Equation for τ_{min} is given in (7), where the minimum is considered for all the possible sign combinations. Compared with a direct numerical search through a 4-dimensional search grid, much less computations – only 16 evaluations of τ – are needed to find τ_{min} with this approach. This allows tag antenna designers to perform rapid worst-case tag performance estimation for a large number of frequency points in practical times.

B. Maximum τ under given impedance tolerances

Treating τ first as a function of the chip impedance only, while considering the antenna impedance fixed, one immediately discovers that the maximum value of τ in Λ_{pq} is one, if the

$$\tau_{min}=\min_{+/-}\frac{4\chi_\varepsilon(1\pm r)\chi_\varepsilon(1\pm p)R_{a0}R_{ic0}}{\left(\chi_\varepsilon(1\pm r)R_{a0}+\chi_\varepsilon(1\pm p)R_{ic0}\right)^2+\left(X_{a0}\pm s\left|X_{a0}\right|+X_{ic0}\pm q\left|X_{ic0}\right|\right)^2}, \quad \chi_\varepsilon(x)=\begin{cases}\varepsilon, & x\leq 0\\ x, & x>0\end{cases} \quad (7)$$

perfect conjugate match impedance point $(R_{a0},-X_{a0})$ is contained in Λ_{pq}. Otherwise, $(R_{ic},X_{ic})\in\Lambda_{pq}$ and $(R_{a0},-X_{a0})\in D/\Lambda_{pq}$ can be joined with a straight line $L(R_{ic},X_{ic})$ crossing the boundary of Λ_{pq}, as illustrated in Fig. 2.

As shown in (4), in $\Lambda_{pq}\subset D$, τ is decreasing towards every direction from the perfect conjugate match impedance point $(R_{a0},-X_{a0})$. From the fact that this holds in particular in the direction along the line $L(R_{ic},X_{ic})$, it follows that in the intersection $L(R_{ic},X_{ic})\cap\Lambda_{pq}$, τ attains its maximum at the boundary of Λ_{pq}. Furthermore, the collection of the subsets of Λ_{pq} for which this is true is actually the whole set Λ_{pq}:

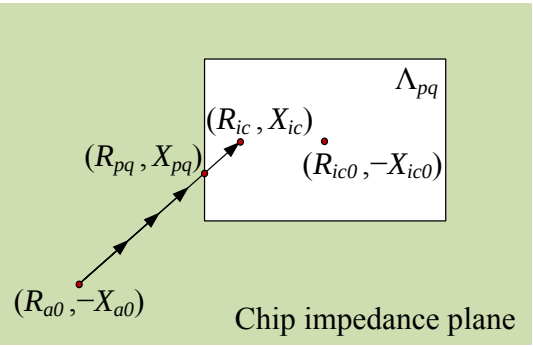


Fig. 2. The perfect conjugate match impedance point joined with a line to an arbitrary point in the chip impedance tolerance rectangle. Arrows indicate the direction of decreasing τ.

$$\bigcup_{(R_{ic},X_{ic})\in\Lambda_{pq}}\left\{L(R_{ic},X_{ic})\cap\Lambda_{pq}\right\}=\Lambda_{pq}. \tag{8}$$

Thus, if the perfect conjugate match impedance point $(R_{a0},-X_{a0})$ is not contained in Λ_{pq}, then the maximum of τ in Λ_{pq} is necessarily attained at its boundary.

Since the expression of τ is symmetric with respect to pairs (R_a,X_a) and (R_{ic},X_{ic}), the same conclusions hold if τ is treated as a function of the antenna impedance, while considering the chip impedance fixed. Based on this observation, a chain of inequalities similar to (6) can be developed as described below.

Let $\partial\Lambda_{pq}$ and $\partial\Lambda_{rs}$ be the boundaries of Λ_{pq} and Λ_{rs}, respectively and suppose that $(R_{a0},-X_{a0})\notin\Lambda_{pq}$ and $(R_{ic0},-X_{ic0})\notin\Lambda_{rs}$. Under these assumptions

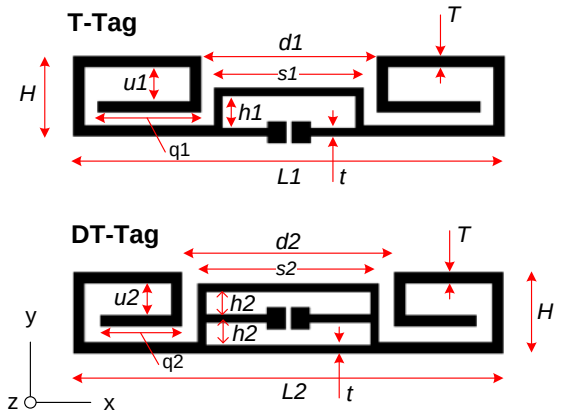
$$\begin{aligned}\tau(R_{ic},X_{ic};R_a,X_A)&\le\tau(R_{pq},X_{pq};R_a,X_a)\\&\le\tau(R_{pq},X_{pq};R_{rs},X_{rs}),\\&=\tau_{max},\end{aligned} \tag{9}$$

for all $(R_{ic},X_{ic};R_a,X_a)\in\Lambda_{pqrs}$, with $(R_{pq},X_{pq})\in\partial\Lambda_{pq}$ and $(R_{rs},X_{rs})\in\partial\Lambda_{rs}$. As the upper bound for τ obtained in (9) is actually the function itself evaluated at a point in Λ_{pqrs}, τ_{max} is necessarily a maximum of τ within this set and it is attained in the Cartesian product $\partial\Lambda_{pq}\times\partial\Lambda_{rs}$. Finally, if $(R_{a0},-X_{a0})\in\Lambda_{pq}$ or $(R_{ic0},-X_{ic0})\in\Lambda_{rs}$, then $\tau_{max}=1$.

Based on this theoretical insight, the maximum of τ under given impedance tolerances can be evaluated much more efficiently compared with a direct numerical search through a 4-dimensional grid, since only a very limited subset – the Cartesian product $\partial\Lambda_{pq}\times\partial\Lambda_{rs}$ – of the 4-dimensional rectangle Λ_{pqrs} needs to be considered. With this approach, e.g. a search grid of size $n\cdot n\cdot n\cdot n$ is reduced to significantly smaller grid of size $4n\cdot 4n$, which means a $1-16/n^2$ relative size reduction.

III. TAG DESIGNS AND SIMULATION RESULTS

The frontend circuitry of an RFID chip is composed of capacitors, diodes and semiconductor switches, making the input impedance of the IC capacitive, as well as frequency and power dependent [11-13]. On the other hand, the input impedance of a short dipole tag antenna, operating below the fundamental resonance frequency of the antenna, is capacitive [2] and needs to be transformed to be inductive in order to conjugate match the tag antenna with the chip. This can be done using T-matching [6-9], which in practice is realized by forming a short circuit current path parallel to the antenna terminals. With the standard (single) T-matching this means adding a conductor loop in the structure around the antenna terminals. With the embedded T-matching, the short circuit current path is formed by a slot, which inscribed in the structure around the antenna terminals. The input impedance of a T-matched short dipole with a fixed length is then controlled by the shape of the short circuit current path. For example, with the commonly used rectangular path, the antenna input impedance can be controlled with only two parameters; the length and width of the rectangle.



	$H = 15$	$T = 2$	$t = 1.5$
T-Tag	$L1 = 80.7$ $d1 = 33$	$h1 = 6.1$ $u1 = 6.5$	$S1 = 28$ $q1 = 19.4$
DT-Tag	$L2 = 80.7$ $d2 = 40$	$h2 = 4.2$ $u2 = 6$	$S2 = 34$ $q2 = 15.4$

Fig. 3. Layout of the designed T-matched tag antenna (top) and double T-matched tag (bottom). Values of the geometrical parameters are in millimeters.

Further degrees of freedom in the T-matching approach may be added by means of multiple T-matching stages [6]. In references [7-8] complex dipole antenna configurations with modified double-T matching approaches have been proposed. On the other hand, the present study focuses on a judicious performance comparison of fairly basic dipole antenna configurations with standard (single) T-matching and its simplest possible extension to double T-matching by addition of another identical loop.

The comparison is done using quarter wave dipole tag antennas with the same foot-print size and very similar radiating geometry. The structure of these tags is shown in Fig. 3. The chip used in both tag designs is the Higgs-3 UHF RFID IC by Alien Technology with the input impedance measured at the wake-up power of the chip [14]. The conjugate of this impedance, i.e. the target for the antenna impedance, is shown in Fig. 4. Ansoft high frequency structure simulator (HFSS) was employed in the antenna design.

Substrate material for the antenna designs is Rogers RT/duroid 5880 with the thickness of 3.175 mm, relative permittivity 2.2, and loss tangent 0.0009. This material was chosen due to its well-known microwave properties to reduce the design uncertainties and thereby yield more reliable comparison between the studied antennas. However, for tag antennas aimed for mass markets, thin low cost plastic films are a preferred choice for antenna substrate.

Since it is known that with the standard T-matching approach, good complex conjugate matching at a single frequency can be achieved, the design goal for the T-matched tag (T-Tag) was good performance within the US RFID band centered at 915 MHz. With the added degree of freedom in the impedance tuning with the double T-matching approach, a broader operational bandwidth is expected of DT-Tag. Therefore, a more challenging design goal with good antenna radiation characteristics together with more than 50% power transfer between the antenna and the chip throughout the global UHF RFID frequencies from 860 MHz to 960 MHz was considered.

The initial simulations showed that in practice, the added degree of freedom in the double T-matching approach manifests itself as a non-monotonic frequency response of the antenna reactance. This achievable feature allows a small dip to be tailored in the antenna reactance response to reduce its total variation over a range of frequencies. The reactance response of T-Tag, however, is inherently monotonic. This suggests that the expected broader operable bandwidth of DT-Tag may be realized by utilizing the local reactance dip in the tag antenna impedance in order to create a dual-frequency impedance matching.

In both tag antenna designs, the spiraled dipole arms are used to increase the electrical size of the antenna through the current alignment principle [4] and thus the fundamental resonance frequency of the antennas is much affected by the shape of the arms. Therefore, the related parameters *H*, *T*, *q1* and *q2* and *u1* and *u2* were first chosen in such a way that the fundamental resonance of the tag antennas with lengths *L1* and *L2* set to 80 mm (close to quarter wavelength) occurred slightly above 1 GHz. In this way, a gradual reactance slope favorable for the design was achieved over the frequencies of interest with both antennas. After this initial step, DT-Tag was optimized for the expected broadband operation, by varying the parameters *L2*, *h2*, and *s2* with *L2*

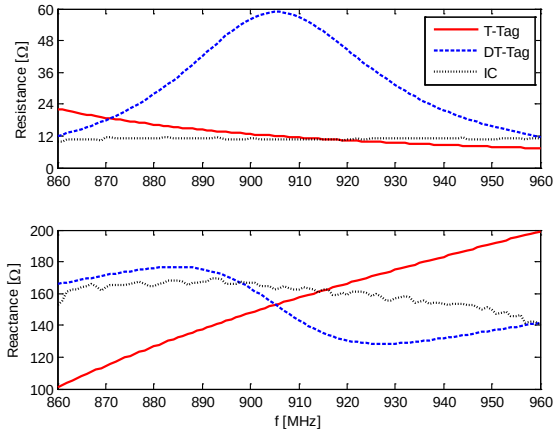


Fig. 4. Simulated tag antenna impedance and conjugate of the measured chip impedance.

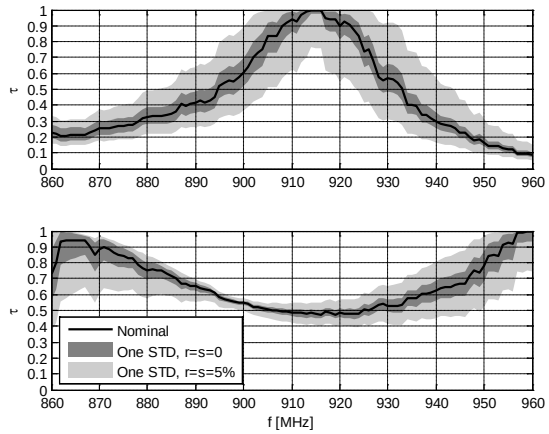


Fig. 5. Power transmission coefficient of T-Tag (top) and DT-Tag (bottom).

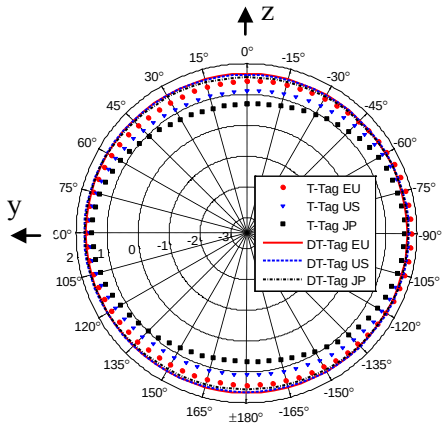


Fig. 6. Simulated tag antenna gain (dBi) yz-plane.

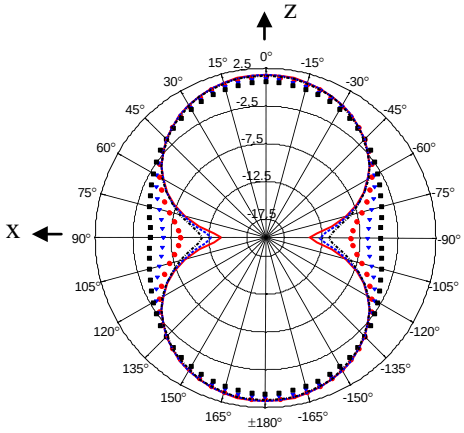


Fig. 7. Simulated tag antenna gain (dBi) xz-plane.

restricted in the neighborhood of the quarter wave length.

Before optimizing the T-matching loop of T-Tag, the parameter *L1* was set equal to *L2* to achieve exactly the same antenna foot-print size for both tags and thereby enable fair comparison between them. Then the parameters *h1* and *s1*, where optimized to satisfy the design goal for T-Tag: good performance within the US RFID band. The built-in genetic optimizer of HFSS version 12 was used in the design.

The optimized antenna impedance of T-Tag and DT-Tag is shown together with the conjugate of the chip impedance (antenna design target) in Fig. 4. The corresponding power transmission coefficients are presented in Fig. 5 with solid "Nominal" curve. These simulation results predict that the T-Tag is well matched near 915 MHz with both resistance and reactance close to their target values. For DT-Tag the same holds in edges of the studied frequency range. In the mid-band, the DT-Tag is also reasonably matched, despite the seemingly large antenna resistance compared with the chip resistance. This is understood by examining the power transmission coefficient given in (2) as a function of the antenna resistance. With small reactance mismatch, the optimal value for resistance is $R_a \approx R_{ic}$, but beyond this value, the increasing numerator $4R_aR_{ic}$ limits the decrease in τ. For reactance mismatch the rate of decrease in τ is determined solely by the square expression in the denominator. This explains the more rapid decrease of τ for the T-Tag, despite the good resistance match in the studied frequency range.

The Monte Carlo simulation method used in the chip impedance measurement [14] gives the chip resistance and reactance as means of Gaussian distributions with known standard deviations. The two uncertainty envelopes shown in Fig. 5 are based on 0% and 5% percentage tolerance in the simulated antenna impedance and the one standard deviation uncertainty for the measured chip resistance and reactance. In order to use the analysis from Section II to calculate the minimum and maximum power transmission coefficient under these impedance uncertainties, the standard deviations were first transformed into percentage tolerances. The envelope minimum is obtained from (7) and the maximum with direct numerical search through the set $\partial\Lambda_{pq}\times\partial\Lambda_{rs}$ defined in Section II.

In Fig. 5, the 0% case (r=s=0) represents a hypothetic perfectly successful simulation-based design and the 5% case (r=s=0.05) represents a more realistic scenario, which could be achieved with good modeling practices. In this study, tolerances beyond 5% were not considered, since the goal of the simulations is to provide judicious performance comparison between the two antennas on a platform with well-known dielectric properties. However, with larger antenna impedance tolerances, the analysis presented in Section II.A can be used for evaluating the platform-tolerance of RFID tags in terms of the minimum τ under variations in the tag antenna impedance when the tag is attached on different items with different electromagnetic properties.

As seen from Figs. 6-7, both antennas have an omnidirectional radiation pattern in yz-plane (the dipole H-plane) and an 8-shaped pattern in xz-plane (the dipole E-plane). Moreover, both antennas are linearly polarized in yz-plane with predominantly x-directed electric field component. It can also be observed from Figs. 6-7, that the gain of T-Tag decreases slightly with frequency in the yz-plane, while the minimum gain in xz-plane is increasing, whereas the gain pattern of DT-tag is less affected by frequency. However, in the yz-plane the gains of the two antennas are of the same order.

These results show that the matching network does not affect much on the radiation properties of the antenna and thus, the comparison of the antennas' performance in terms of the matching approach is fair.

All the tag measurements discussed in the next Section were conducted in the forward direction corresponding to the direction of the z-axis in Figs. 6-7. In this particular direction, the forward gain of DT-tag is found to be approximately constant at 1.6 dBi, while for T-Tag, the gain decreases from 1.5 dBi at 860 MHz to $G_{fwd} \approx 0.7$ dBi at 960 MHz.

IV. MEASUREMENT RESULTS AND DISCUSSION

In order to verify the tag designs experimentally, the simulated and measured empty space read range is compared. Here it is assumed that the read range is limited by IC's wake-up power and Friis' simple transmission equation [15] is used in the calculations. This simple formulation may not be sufficient for estimating the read range in complex real-life environments [16] and in some applications with strong tag-to-tag coupling the receiver sensitivity may be limiting the read range [17]. However, in a controlled measurement environment, the empty space read range allows direct comparison between the measurements and simulations and thereby provides a method for design verification. In the present study, the main goal of the experimental work is to add assurance for the simulation-based conclusions about the performance of the compared tags.

To characterize the forward link performance of the designed tags experimentally, the transmitted threshold power (P_{th}) was measured for each tag. This is the minimum transmitted continuous wave power at which a valid response to Electronic Product Code (EPC) Generation 2 protocol's *query* command is received from the tag under test. The threshold measurement was conducted in the forward direction in a compact anechoic cabinet with a linearly polarized transmitter antenna. During the measurement, the tag antennas were carefully aligned to match the polarization of the reader to minimize the link loss due to polarization mismatch. In addition, the path loss (L_{fwd}) from the generator's output port to the input port of an equivalent isotropic antenna placed at the tag's location was measured using the calibration procedure of the measurement device. This allows the compensation of any possible multipath effects in the measurements space, as described below.

According to Friis' simple transmission equation:

$$P_{ic,sens} = \tau G_{tag} L_c G_{tx} \left(\frac{\lambda}{4\pi d} \right)^2 P_{th^*}, \qquad (10)$$

where $P_{ic,sens}$ is the wake-up power of the chip, P_{th^*} is the equivalent transmitted threshold power that would be measured in the perfect empty space conditions, L_c is the cable loss from the generator's output (matched to the cable) to the input port of the transmitting antenna (matched to the cable), the gain of the transmitting antenna and the tag antenna are G_{tx} and G_{tag}, respectively, and the separation between these antennas is d. On the other hand, in the real measurement it holds

$$P_{ic,sens} = \tau G_{tag} L_{fwd} P_{th}. \qquad (11)$$

Thus, multiplying the measured transmitted threshold power with the factor Λ defined as

$$P_{th^*} = \Lambda P_{th}, \quad \text{with} \quad \Lambda = \frac{L_{fwd}}{L_c G_{tx} \left(\frac{\lambda}{4\pi d} \right)^2}, \qquad (12)$$

the measured P_{th} is mapped to the value that would have been obtained in empty space.

On the other hand, assuming that the measurement was conducted in empty space, the theoretical read range is

$$\begin{aligned} d_{tag} &= \frac{\lambda}{4\pi} \sqrt{\frac{\tau G_{tag} L_c G_{tx} P_{tx,EIRP}}{P_{ic,sens}}} \\ &= \frac{\lambda}{4\pi} \sqrt{\frac{\tau G_{tag} L_c G_{tx} P_{th^*}}{P_{ic,sens}}} \sqrt{\frac{P_{tx,EIRP}}{P_{th^*}}} \\ &= d \sqrt{\frac{EIRP / G_{tx} / L_c}{P_{th^*}}}, \end{aligned} \qquad (13)$$

where $P_{tx,EIRP}$ is the transmitted power corresponding to the regulated equivalent isotropically radiated power (*EIRP*). The theoretical empty space read range is now obtained by expressing P_{th^*} in terms of P_{th} and L_{fwd} from (12) and substituting this into (13). As a result we get,

$$d_{tag}^{\,m} = \frac{\lambda}{4\pi} \sqrt{\frac{EIRP}{L_{fwd} P_{th}}}, \qquad (14)$$

where the superscript *m* indicates that this value is based on measurements.

For comparison between the measurements and simulations, the theoretical empty space read range can be calculated with Friis' simple transmission equation using the simulated power transmission coefficient (τ), tag antenna gain in the forward direction (G_{fwd}), and the chip sensitivity ($P_{ic,sens} = -18$ dBm) provided by the manufacturer. Under these definitions, the simulated value is given by

$$d_{tag}^{\,s} = \frac{\lambda}{4\pi} \sqrt{\frac{\tau G_{fwd} EIRP}{P_{ic,sens}}}. \qquad (15)$$

Comparison of the measured and simulated theoretical empty space read ranges with European power regulation (EIRP = 3.28W) is shown in Fig. 8.

Simulation results, in Figs. 4-5, predict good reactance matching for DT-Tag at both ends of the studied frequency range, while the tag antenna gain was observed to remain approximately constant. This agrees with the measured frequency response shown in Fig. 8, with peak performance at the edges of the measured frequency range and slightly weaker performance in the middle. The simulated reactance of T-Tag, shown in Fig. 4, increases monotonically through the studied frequencies and consequently, good conjugate impedance matching is achieved only in the neighborhood of 915 MHz. This agrees with the measured frequency response, shown in Fig. 8. Simulations also predict a decreasing slope in the tag antenna gain versus frequency, which agrees with the measured frequency response as well; T-Tag's performance decays faster towards the higher end of the measured frequency range. In addition, both tag antenna designs are verified within 5% impedance tolerances through the majority of the studied frequency points. This provides further assurance for the performance comparison between them.

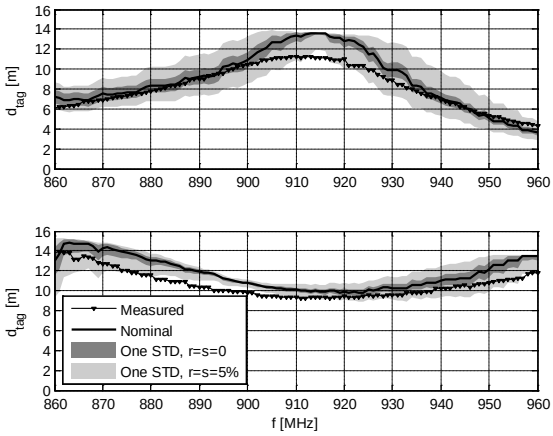


Fig. 8. Theoretical empty space read range of T-Tag (top) and DT-Tag (bottom) in the forward direction.

V. CONCLUSIONS

The impact of tag antenna and chip impedance tolerances on power transfer between these components was investigated analytically. Means for efficient computation of the minimum and maximum power transmission coefficient under given impedance tolerances were developed and a closed-form expression for the minimum value was derived. This analysis provides tools for tag antenna designers to validate their designs.

The presented sensitivity analysis was employed to quantify the design uncertainty of single and double T-matched short dipole tags. Both, the simulation-based and experimental comparisons of these tags showed that the bandwidth of a standard T-matched tag can be significantly improved with the double T-matching approach. Importantly, the modification of the standard T-matching to double-T matching requires only a minimal structural modification, which in our study did not increase the antenna foot-print size.

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