Optimization of Transmission Line Discontinuities using the Genetic Algorithm

J. Alan Roden
Electromagnetic Consultant Engineer

Raleigh, NC 27614
Email: Alan.Roden@IEEE.ORG

Abstract. In this paper, a genetic algorithm based optimization procedure is applied to the equivalent circuit optimization of a microstrip via. A new form of equivalent circuit is introduced which more accurately characterizes the vias' performance. Spice results are presented which demonstrate the impact of various via topologies on transmission line signal integrity.

I. Introduction

Accurate three-dimensional electromagnetic analysis of complex systems oftentimes exceeds the analysis capabilities of modern-day computer systems. Subsequently, the signal integrity or packaging engineer must rely on intelligent simplifications of the problem scenario in order to minimize the computational requirements. One such scenario is the modeling of uniform transmission lines using one-dimensional transmission line techniques such as those in Spice. In the regions where a uniform transmission line exists, TEM assumptions are valid, and simple transmission line analysis methods may be applied accurately. It is in such a manner that most complex systems are modeled today.

When discontinuities are encountered along a transmission line, TEM field assumptions are no longer valid and a pure transmission line modeling approach can lead to significant error. In such a scenario, a full-wave approach is needed to accurately characterize the electromagnetic effects of the anomaly. Full wave analysis of an entire PCB design is typically not practical due to computational and time demands. Furthermore, device libraries for the various active components which exist on a printed circuit board are typically only available in a Spice-like environment.

A good compromise approach entails the incorporation of lumped-parameter equivalent circuit models to capture the three-dimensional effects of the discontinuity. In such an approach, the full wave analysis engine is *only* applied to the discontinuity whereas a Spice equipped circuit solver is applied to the majority of the problem domain where TEM field assumptions are valid, ie the uniform regions of the system's transmission lines. Such an approach yields an accurate and efficient solution to many complex modeling problems.

Equivalent circuit design does not provide an exact solution. The discontinuities which are to be modeled typically do not have an exact analytic solution. Therefore, an optimal solution over a desired frequency band must be the goal. Numerous optimization techniques may be employed.

Here, the genetic algorithm is employed due to its robust capabilities and its ease of use. It does not typically suffer the most typical problem of getting trapped in non-optimal local minima.

In this paper, the genetic algorithm is applied along with the FDTD technique in order to derive an accurate broadband equivalent circuit for a microstrip via. In section II, a design and optimization procedure will be presented. In Section III, results are demonstrated for two commonly occurring microstrip via topologies. Finally, the paper is concluded in section IV.

II. Equivalent Circuit Extraction Using the FDTD Technique

The equivalent circuit generation procedure used here is similar to that reported by Werner and Mittra[1]. Initially, the n-port scattering matrix is extracted from the discontinuity over the frequency domain of interest. Here the scattering parameters are computed from a full-wave solution using the finite-difference time-domain technique (FDTD) . Subsequently, an equivalent circuit form is chosen to represent the discontinuity. It is essential that the circuit has adequate complexity to fully characterize the discontinuity over the frequency band of interest. Next, the scattering parameter matrix of the proposed equivalent circuit is developed analytically. Finally the genetic algorithm is applied to optimize the R, L, and C parameter values of the proposed equivalent circuit so as to match the characteristics of the measured scattering parameters.

The FDTD technique is uniquely qualified to determine scattering parameters from discontinuities for several reasons. First, the FDTD solution is a broadband solution, therefore all necessary frequency components are computed from one simulation. Second, a most unique characteristic of the FDTD technique as opposed to other integral equation based techniques such as the method of moments, is its use of absorbing boundaries. Specifically, absorbing boundaries are used to terminate the problem domain.

For the present case, the PML absorbing boundary condition was employed which has very robust absorption performance over a wide frequency band [2],[3]. At normal incidence, less than -100dB of reflection error can be expected. This excellent ABC performance allows the computational domain to be truncated very close to the discontinuity, thus limiting the problem size. Additionally, for printed circuit board geometries, the PCB may be extended through the PML region. The effect is to emulate an infinite reference plane in each dimension. Thus, the problem solution is immune from resonant effects which finite reference planes will introduce. For discontinuities which produce very small perturbations, such resonances can completey invalidate the scattering parameters computed.

Recently, much research has been directed at producing accurate broadband equivalent circuits using purely analytic methods in an automated manner[4]. In some cases, a simple cascading of ‘pi’ or ‘T’ networks may be adequate. Currently, however, choosing an accurate and efficient equivalent circuit topologies still requires good engineering insight. The success of this procedure is highly dependent on how well a circuit topology can match the discontinuity behavior over the frequency band of interest.

The optimization procedure accomplishes a minimization of the distance between the actual measured or simulated S parameters and the S parameters of the equivalent circuit posed. Mathematically, this is stated as

$$C = \sum_{n=1}^{nfreqs} \sum_{i=1}^{N} \sum_{j=1}^{N} \left| S_{ij}^{meas}\left(f_n\right) - S_{ij}^{equiv}\left(f_n\right) \right|^2 . \quad (1)$$

The function C is referred to as the cost function. The minimization of this function is the duty of the genetic algorithm. The genetic algorithm[5] is an optimization procedure based on the 'survival of the fittest'. Each circuit parameter is represented by n-bit string called a *gene*. Groups of *genes* are referred to as a chromosome, where a chromosome represents one individual design within the population. Initially, a parameter value range is chosen for each gene (circuit element). The genetic algorithm starts with an initial population of designs. Subsequently, chromosomes(designs) are mated and mutated providing new populations at subsequent generations. The designs in each generation are graded against the cost function, and the most robust design characteristics are carried to future generations. Through such an evolutionary process, after a fixed set of generations, an optimal design is achieved.

It is important to note that the design resulting from this design process is an *optimal* design given the circuit topology and parameter range supplied. If the circuit topology does not adequately describe the frequency behavior of the discontinuity, the resulting optimized circuit will not accurately represent the problem. Therefore, it is crucial that a proper equivalent circuit topology be posed.

III. Example: The Microstrip Via

The microstrip via is a common and crucial design element in most modern-day printed circuit board designs. It is also common within chip packages where numerous voltage and reference planes exist. A via provides an electrical path for a signal to transverse between various wiring planes within a PCB or package substrate. The via can extend entirely through the board regardless of the layer of the signal and reference layers, or can simply exist between the two layers where the signals is transversing (blind via). The first of these is studied here although a similar analysis and model can be applied to the blind via as well.

The via is characterized by its barrel size, annular ring size, and clearance dimension on each layer. The barrel is cylindrical and extends the through the height of the board, the annular ring exists at the top and bottom of the via minimally, but also at each layer where a signal line is connected. The clearance area is a cylindrically drilled hole which creates an isolation area around the via from adjacent materials.

All vias are not the same from an electrical standpoint. The two major classifications of vias are the simple via and the through-board via. The simple via electrically connects signal traces on the opposing layers of a common reference plane. For such a via, the return current has a

continuous current path through the clearance hole in the reference plane to the opposite side of the reference plane, where the completion of the signal circuit exists. The through-board via traverses numerous reference layers moving from one initial reference plane to a final different one.

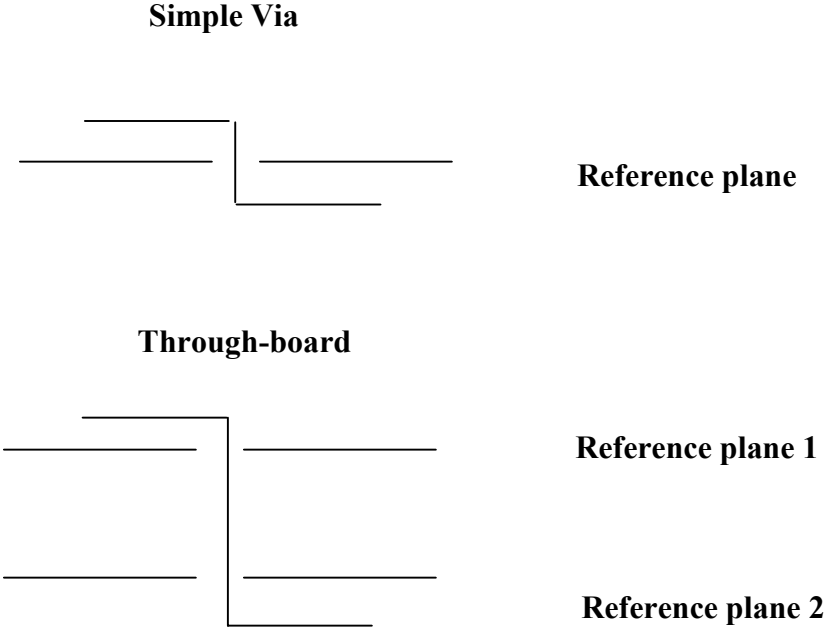

Figure 1 Common via topologies for printed circuit boards.

Initially, a full-wave analysis of the via is accomplished using the FDTD technique in order to determine its scattering parameters. The first geometry analyzed consists of a 50 ohm trace, a through-board via (barrel=10mil diameter, annular ring 20mil diameter), followed by another 50 ohm trace on the opposite sidee of the board. The trace is doubly terminated into the PML absorbing boundary. The board core is 60 mils thick. Two ground vias of equivalent dimension are placed 100 mils from the signal via on either side of it. These represent decoupling capacitors which would be present in a real design. It is important to note that decoupling capacitors are not typically placed this close to every signal line, therefore the performance here is a bit ideal.

The discretization is 2 mils in each dimension. The problem dimension is 80 x 200 x 50. The microstrip is excited by a gaussian pulse with a bandwidth of 5 GHz. Port 1 is defined 50 mils from the via on the top layer, port two is defined 50 mils from the via on the bottom layer. Time domain voltages are measured at each reference plane with and without the via present. Subsequently, scattering parameters are computed effectively with reference plane shifts to give parameters of the vias alone.

Figure 2 illustrates the time domain waveforms at port 2. Clearly some time shift does occur as well as some signal amplitude distortion. Looking closely, we see some loss. This is primarily due to the radial wave launched internal to the board, but also to the return loss. An equivalent circuit was derived based on previous work as well as the insight gained from simulations and

viewing subsequent field animations. The initial circuit chosen was a multi-stage 'pi' circuit where the number of stages could be varied. The circuit was similar to that used by Harms in [6]. It was determined that this model could be modified slightly to give better performance for the through board via. The additions accounted for the plane-to-plane capacitance and inner plane loss through components R3 and C3. This modified T circuit is shown in Figure 2.

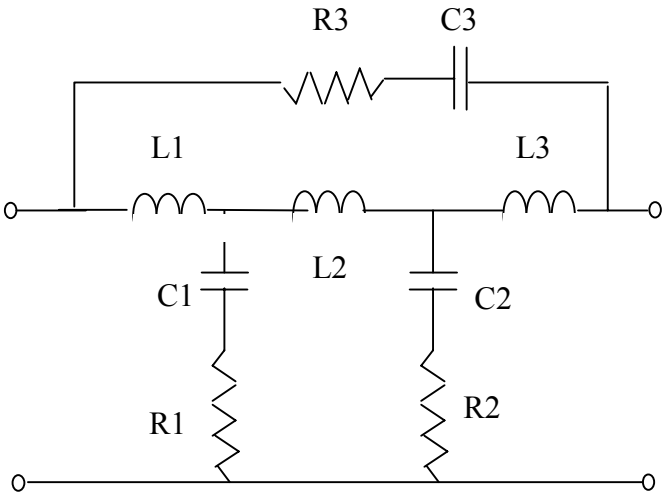

Figure 2 Equivalent circuit for PCB via; modified 'T' design.

Figure 3 illustrates the time domain voltage waveform at port 2 for the through board via. Clearly, the most significant effect is the phase shift which will be board thickness dependent.

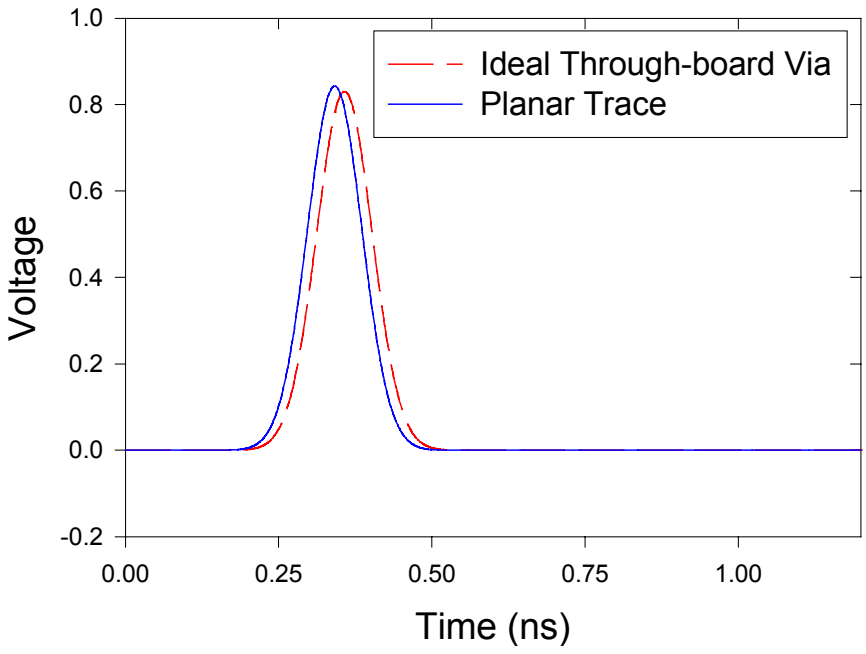

Figure 3 Time domain FDTD waveform at port 2 for a through board via.

In Figure 4 the scattering parameters S_{11} and S_{21} are illustrated. Here the initial two-stage 'pi' design, the modified 'T' design, and the measured results are shown. Clearly, good agreement

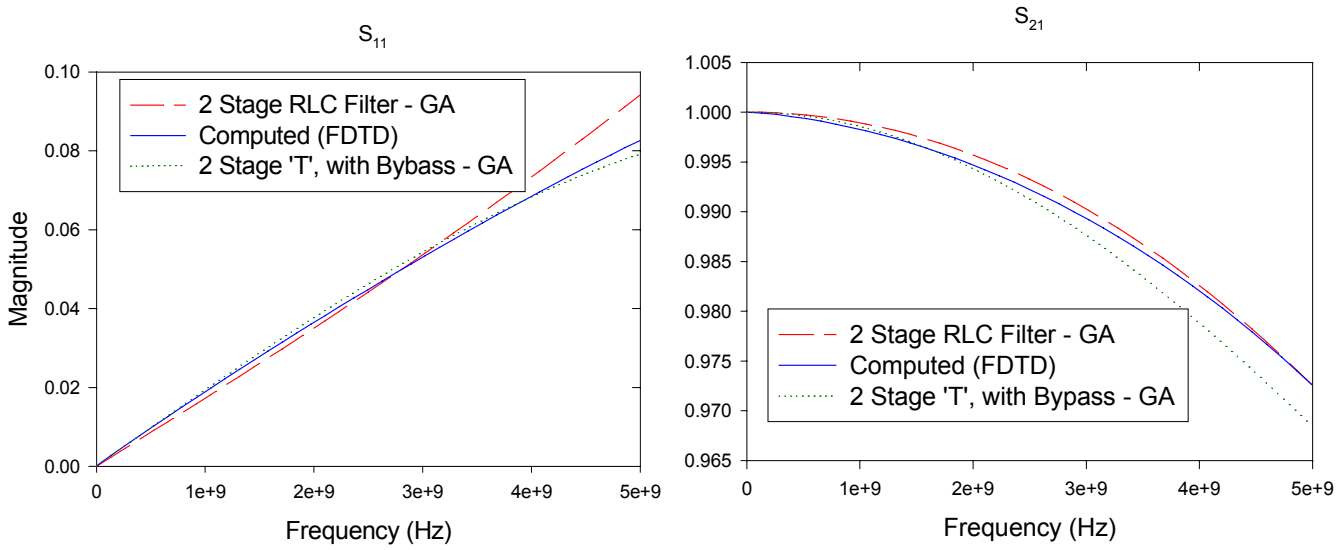

Figure 4 Magnitude of Scattering parameters for through board via. (unitless)

exists across the entire band with some deviation by the simple two stage 'pi' above 3 GHz. Similarly, the phase is shown in Figure 5. Here, we see again that the S_{11} phase performance for the new modified 'T' design is excellent with some error from the 2 stage 'pi' design. The phase of S_{21} showed good agreement for either model. It is important to note that the complexity of the 'pi' circuit was increased to as large as eight stages in an attempt to get better broad band performance. Such efforts led to no further improvement.

Figures 5 and 6 represent the culmination of the equivalent circuit design. Here the genetic algorithm generated equivalent circuits are included in a Spice simulation of an ideally terminated transmission line. Also included in these plots is a simple and commonly used model for a via, a 1 pF capacitor. This trusted model has been used for years due to its simplicity.

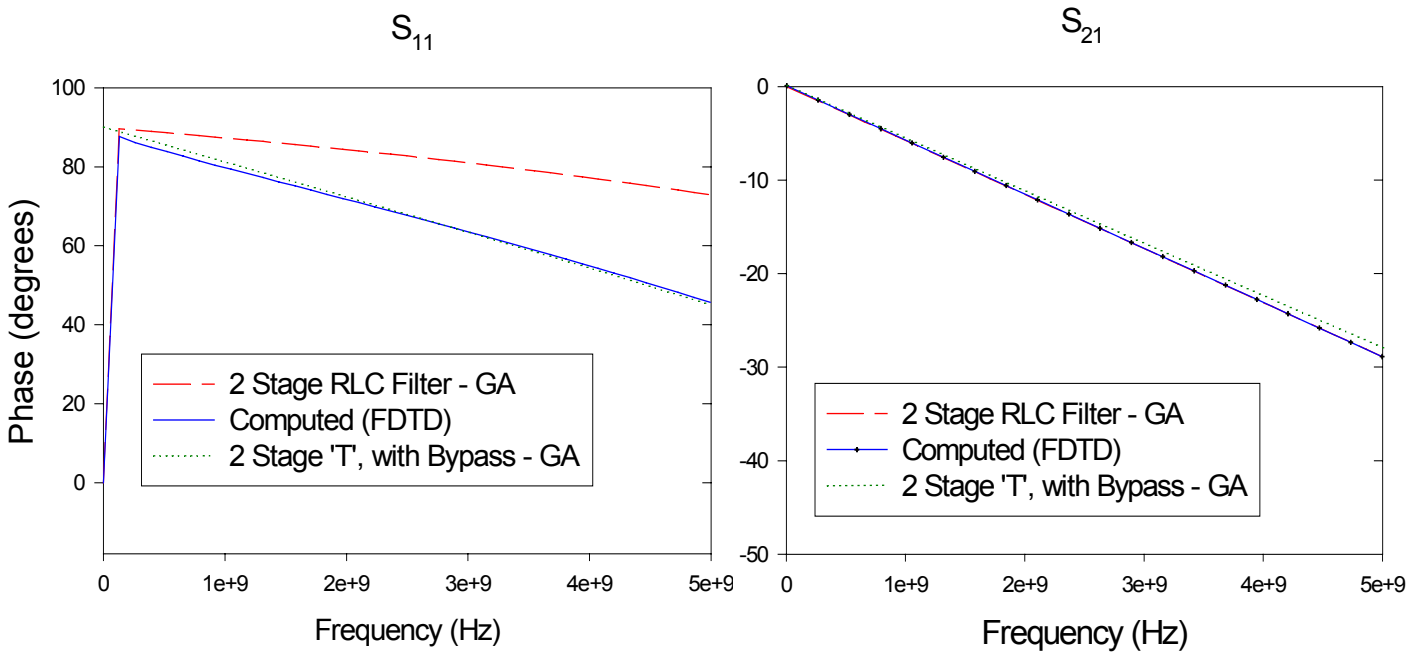

Figure 5 Scattering parameter phase for through board via.

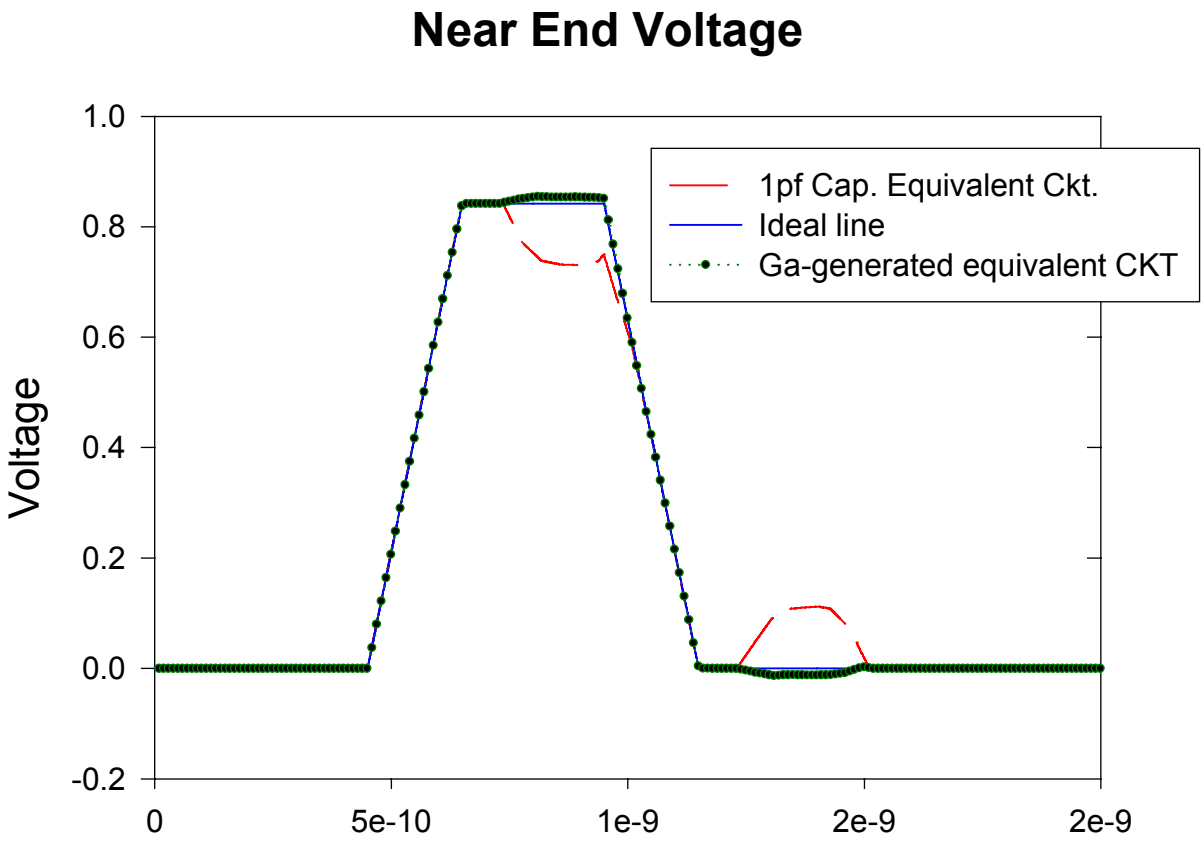

Figure 6 Spice simulated near-end voltage including genetically designed equivalent circuit for a through-board via and a simple 1 pF model for via.

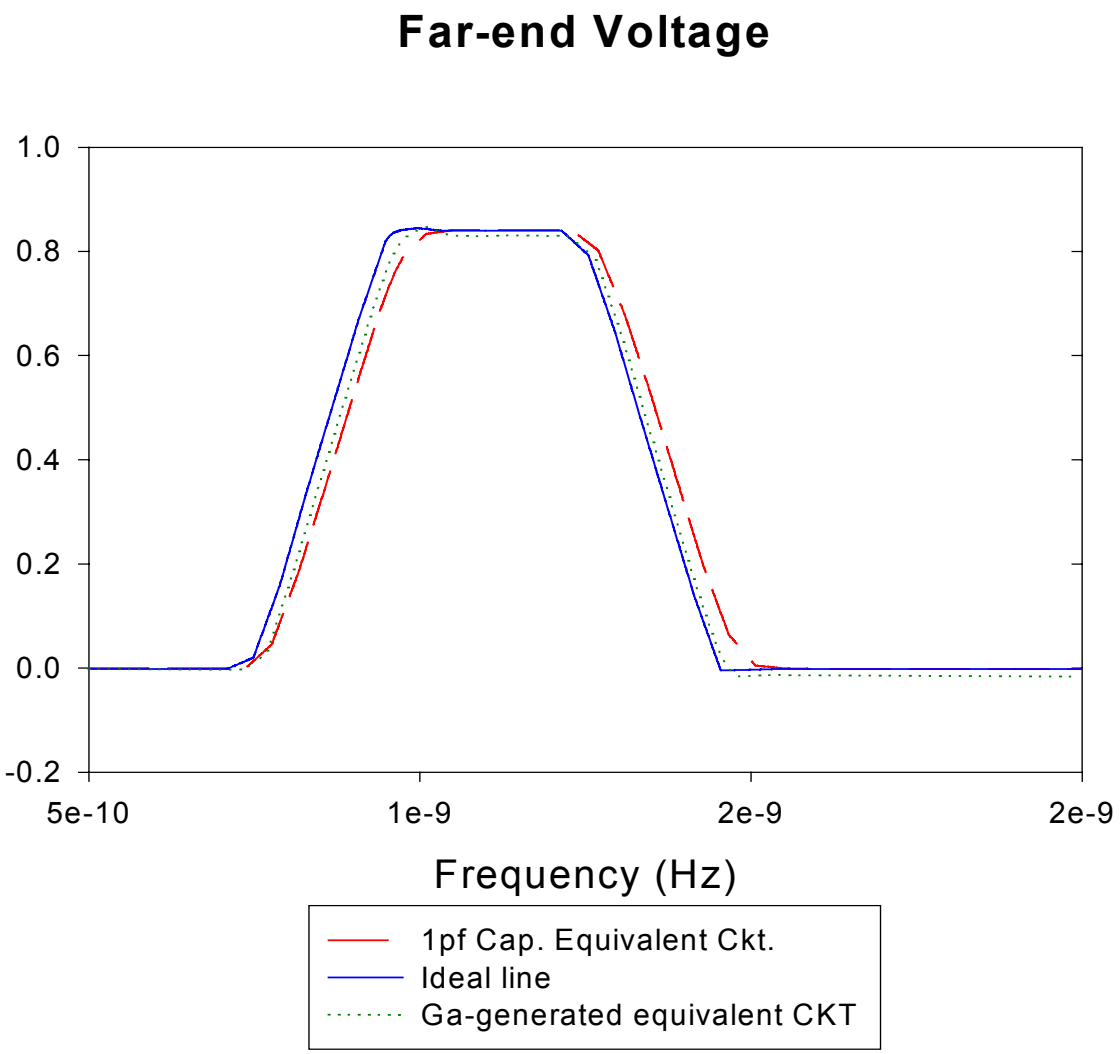

Figure 7 Spice result for far-end voltage for genetically designed equivalent circuit for a through-board via and a simple 1 pF via model.

Figure 5 illustrates that the via does cause a noticeable distortion to the time domain waveform. Interestingly, the actual via model shows much less return loss than the simple 1 pF model of the via. Figure 6 illustrates the primary impact of the microstrip via; delay. Here we see that a delay of about 16 ps is caused by the via. This is a small but significant delay for modern-day designs. Also note that the simple 1 pF cap demonstrated very similar performance to the equivalent circuit with respect to delay, suggesting that this has not been such a bad choice for this most crucial figure of merit.

The simple via was also examined using the current technique. It was found that the simple via produced much less distortion and delay than the through-board via. This is due to the fact that the return current path is not discontinued completely, just rerouted. The genetic algorithm proved to be even more robust for equivalent circuit optimization in this case. The time-domain spice waveform is shown in Figure 7 for the simple via. As is demonstrated here, the delay is greatly reduced over the through-board via (6 ps). Also, the simple capacitor model continues to portray a delay of about 22 ps which is far greater than actual.

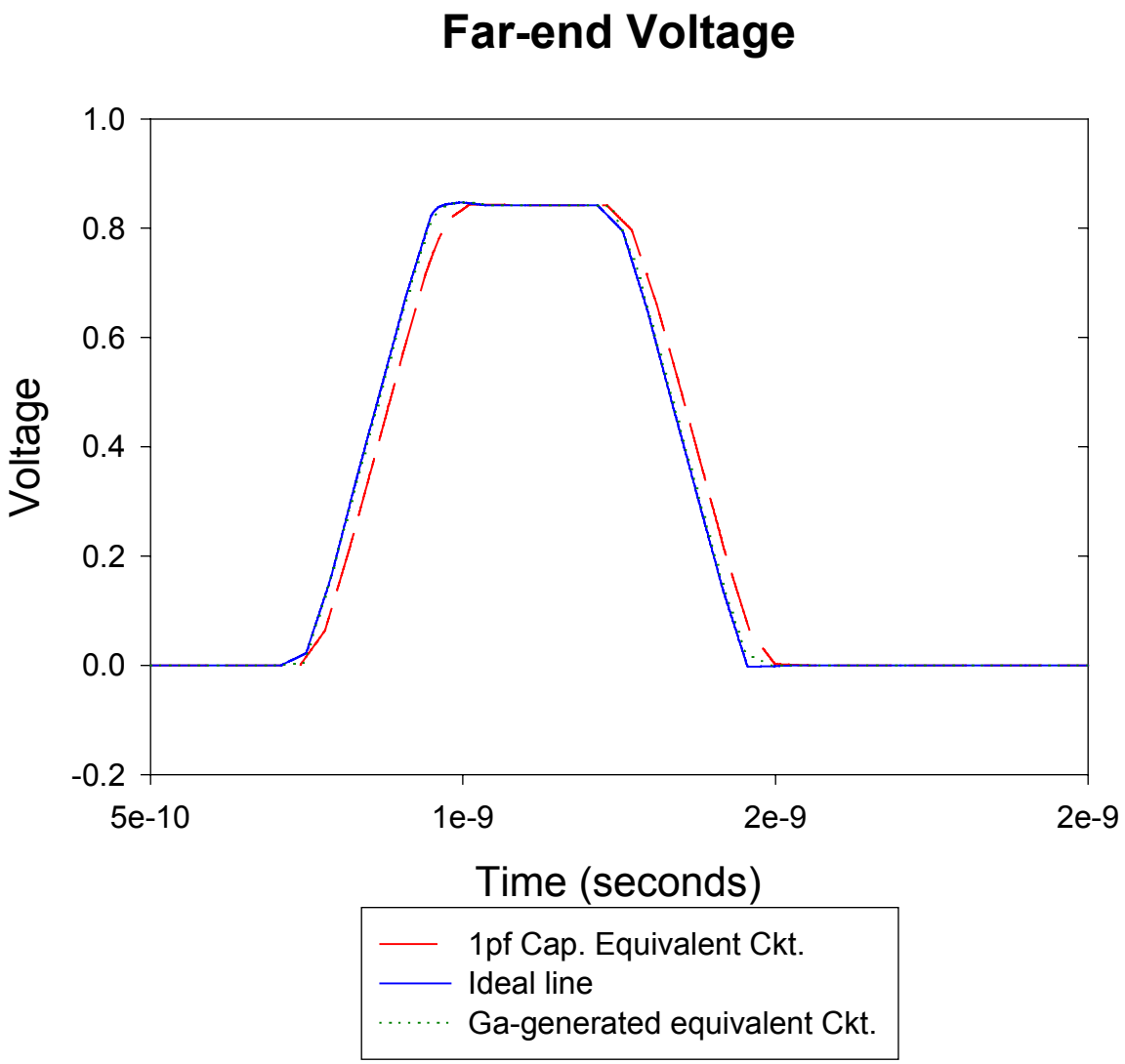

Figure 8 Far-end Hspice voltage for simple via and 1pf capacitor model.

IV. Conclusion

In this paper, the genetic algorithm was applied to the equivalent circuit design and analysis of a via. The results presented showed that the genetic algorithm is indeed a very robust tool for equivalent circuit optimization. Successful equivalent circuit optimization requires an accurate choice of circuit topology. In this work, a new circuit topology was introduced for the microstrip via which proved more accurate than those previous presented. This method may be applied to a variety of geometries where the features are small with respect to a wavelength. Further research is needed to find a systematic method to determine equivalent circuit topologies.

---

[1] P.Werner, R. Mittra, D. Werner, "Extraction of Spice-type Equivalent Circuits of Microwave Components and Discontinuities using the Genetic Algorithm Optimization Technique", *IEEE Transactions on Advanced Packaging*, February, 2000.

[2] Berenger, J P, "Perfectly matched layer for the absorption of electromagnetic waves", *J. Computational Physics*, Vol. 114, 1994, pp. 185-200.

[3] J. A. Roden, Stephen Gedney, "Convolutional PML (CPML): An Efficient FDTD Implementation of the CFS-PML for Arbitrary Media", *Microwave and Optical Technology Letters*, Vol. 27, No. 5, December, 2000.

[4] An Efficient Systematic Approach to Model Extraction for Microwave Integrated Circuits", IEEE Trans on Microwave Theory and Techniques, vol. 48, no 9, September, 2000,

[5] D. E. Goldberg, *Genetic Algorithm in Search, Optimization, and Machine Learning*, Reading, MA, Addison-wesley, 1989.

[6] Harms P, J.-F. Lee, and R.Mittra, "Characterization of the cylindrical via discontinuity", *IEEE Trans Microwave Theory and Techniques*, Vol. 41, 1993, pp. 153-156.