A Broadband Microstrip-to-Microstrip Vertical Via Interconnection for Low Temperature Co-Fired Ceramic Applications

Yupeng Liu, Lei Xia*, and Ruimin Xu

Fundamental Science on EHF Laboratory
University of Electronic Science and Technology of China, Chengdu, 611731, China
lypscottabcd@gmail.com, xialei@uestc.edu.cn*, rmxu@uestc.edu.cn

Abstract ─ This letter presents a microstrip-to-microstrip vertical via interconnect in microwave low temperature co-fired ceramic (LTCC) technology. According to the simulation results, the insertion loss is less than 0.33 dB and the return loss is greater than 29.9 dB from 0.3 GHz to 18 GHz. An equivalent lumped model is developed for analyzing the microstrip-to-microstrip vertical interconnection. The structure has been manufactured and measured.

Index Terms ─ Equivalent model, low temperature co-fired ceramic, microstrip-to-microstrip and vertical via interconnect, microwave.

I. INTRODUCTION

Low temperature co-fired ceramic (LTCC) is in the core place of multi-chip module (MCM) technology. With the excellent RF performance, the recent research shows that LTCC technology is more for use in microwave and millimeter-wave applications, the high-speed high-density, three-dimensional integration technology and so on, by its advantages, such as low thermal conductivity, high packaging flexibility, high integration density, high stability, and low cost [1-3]. It is widely applied in wireless communication systems [4]. Microwave components like stripline, cavity, substrate integrated waveguide (SIW) can be easily implemented on account of its three dimensional (3D) multi-layer structure [5]. LTCC multilayer circuit strctures require the interconnection of signals between different layers which will restrict the overall performance of the circuit systems. This is of key importance in the design of LTCC circuit systems. The high quality LTCC vertical interconnection plays an important role in system-in-package (SiP) module packaging applications. Since the geometry of vertical interconnections have significant effect in the electromagnetic behaviors of the LTCC multi-layer system [6], it becomes necessary to investigate the characteristics of these vertical interconnections.

The detailed design and implementation of the microstrip-to-microstrip vertical interconnection with better performance at microwave frequencies are considered in LTCC technology.

II. DESIGN DESCRIPTION

The configuration of microstrip-to-microstrip single vertical via interconnect is shown in Fig. 1 (a). The bottom microstrip line is vertically connected by coaxial-like signal via hole to microstrip line on top of the substrates. The inner ground planes on three different substrate layers are connected by the staggered via holes.

The proposed structure consists of eight layers of Ferro-A6M substrates with via holes formed by Ferro CN33-407 silver paste, internal conductors formed by Ferro CN33-398 silver paste, and external conductors formed by Ferro CN33-391 silver paste. Each substrate has a thickness of 94 μm with a relative permittivity of 5.9. So the total thickness of the design structure is 752 μm, and the thickness of the external conductors is 10 μm. According to the LTCC process specifications, two ceramic substrate layers are chosen for each microstrip line, which provides reasonable size for 50 Ω transmission lines. Both of the top and bottom microstrip lines are 310 μm conductor in width. The circular pad, connecting the microstrip line and transmission via hole, has a diameter of 320 μm. The height of signal via hole corresponds to the 8-layer LTCC substrate thickness. All via holes in the design are of 130 μm diameter.

In addition, the dominant mode of the microstrip line is quasi-TEM mode. This mode, relative to symmetry plane of the central microstrip line, is an even mode. Besides, the dominant mode of the coaxial-like line, formed by the vertical signal via and the surrounding shielded holes, is TEM mode. And this mode is also an even mode relative to symmetry plane of the central microstrip line. Therefore, it can realize a transition from the quasi-TEM wave of the microstrip line to TEM wave of the coaxial-like line among the interconnection structure. Figure 1 (b) illustrates 3D view of the coaxial-like via structure. As is known to all, the discontinuity effect of the vertical via hole can result in non-negligible signal reflection, which may seriously degrade the performance. Therefore, the effect of characteristic

Submitted On: October 12, 2015
Accepted On: January 24, 2016

impedance on transmission performance is mainly discussed below.

The original characteristic impedance of microstrip line is:

$$Z_0 = \sqrt{\frac{L_0}{C_0}}. \quad (1)$$

In order to improve the signal transmission performance, several ground-shielded via holes are employed around to enhance impedance matching. Meanwhile, the signal via hole produces the parasitic inductance ΔL. The characteristic impedance of vertical signal via hole becomes:

$$Z = \sqrt{\frac{L_0 + \Delta L}{C_0}}. \quad (2)$$

Therefore, in order to achieve impedance matching, we connect microstrip line to signal via hole through a pad, which introduces the compensation capacitor ΔC.

The characteristic impedance then becomes:

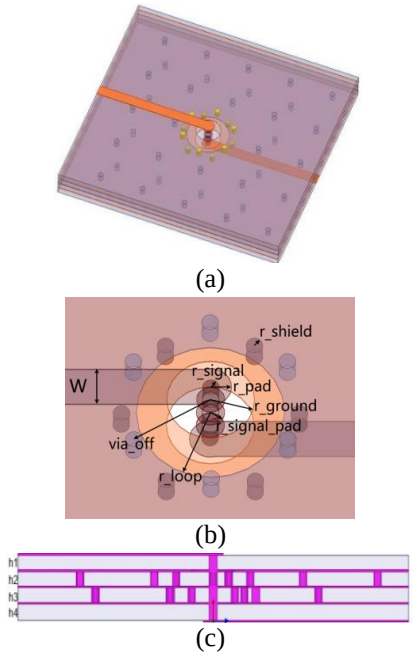
$$Z = \sqrt{\frac{L_0 + \Delta L}{C_0 + \Delta C}} = \sqrt{\frac{L_0}{C_0}} = Z_0. \quad (3)$$

The compensation capacitor ΔC can be directly derivable from the Equation (3):

$$\Delta C = \frac{L_0 + \Delta L - Z_0^{\,2} C_0}{Z_0^{\,2}}. \quad (4)$$

Figure 1 (c) gives the cross sectional view. The parameters of this structure are shown in Table 1. The proposed structures (single and back-to-back) are simulated and carefully tuned in HFSS from 0.3 GHz to 18 GHz. The simulated results of S_{21} and S_{11} are shown in Fig. 2. It can be noticed from Fig. 2 (a) that the insertion loss ($|S_{21}|$) of single vertical interconnection is less than 0.202 dB up to 18 GHz, and the return loss ($|S_{11}|$) is better than 33.79 dB up to 18 GHz. From Fig. 2 (b), it can be observed that $|S_{21}|$ of back-to-back structure is less than 0.33 dB up to 18 GHz, and $|S_{11}|$ is better than 29.9 dB up to 18 GHz.

The improved structure in this letter can achieve better impedance matching and better signal integrity of TEM by the added middle ground plane with the aperture of the anti-pad. In practical manufacturing of LTCC, multi-layer vertical vias are easy to cause dislocation, which can affect signal connectivity. In particular, a disconnected signal via leads to microwave performance deterioration. Therefore, in order to prevent the impact of vertical via dislocation on performance, the surrounding shielded holes and the added middle ground plane with the aperture of the anti-pad are added to ensure better signal integrity of TEM in the event of slight dislocation. Therefore, it is observed that the proposed interconnect structure has better transmission performance. From the result of this work, it can be suggested that this interconnect structure is more suitable for vertical interconnection applications of microwave LTCC integrated circuit and SiP module packages.

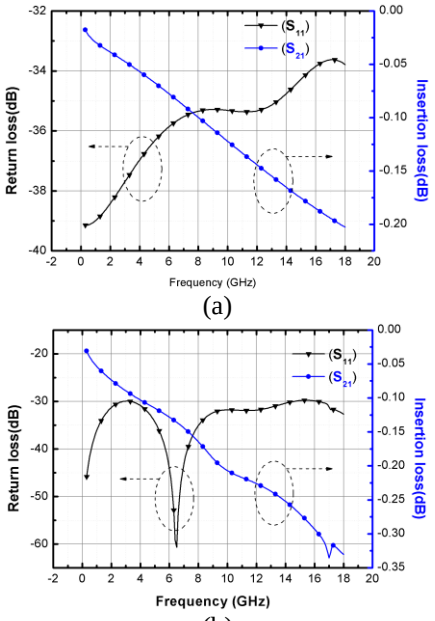


(a)

(b)

(c)

Fig. 1. The overall structure of microstrip-to-microstrip vertical via interconnects: (a) 3D view (single vertical interconnection), (b) coaxial-like via structure, and (c) cross sectional view for via interconnect.



(a)

(b)

Fig. 2. Simulated S_{21} and S_{11} responses of microstrip-to-microstrip vertical interconnect: (a) single vertical transition, and (b) back-to-back structure.

Table 1: The parameters of this structure

Structure Parameters	Quantity	Data (mm)
W	Microstrip width	0.31
r_pad	Radius of pad connecting microstrip line to signal via	0.16
r_signal_pad	Radius of pad for signal via	0.11
r_signal	Radius of signal via	0.065
r_shield	Radius of shield via	0.065
r_ground	Radius of opening in microstrip ground plane	0.34
r_loop	Radius of opening in middle ground plane	0.575
via_off	Distance between shield via and signal via	0.69
h_i	Substrate thickness (h_1, h_2, h_3, h_4)	0.188

III. EQUIVALENT TRANSITION MODEL

An improved equivalent circuit, which is deduced theoretically from reference [7], is used for analyzing vertical via in Fig. 3. The impedance, inductance and capacitance effects of vertical via holes are considered. Hence, it consists of a seven lumped elements pi-equivalent circuit model for the single vertical via interconnect. L_1, C_1 and R_1 denote parasitic inductance, capacitance and resistance of vertical via respectively. R_2 and C_2 represent the parasitic resistance and capacitance between pads of vertical via holes and adjacent ground planes [8-10].

The equivalent model has been optimized and tuned in Agilent ADS on the parameters of the simulation result. The model parameters are extracted and listed in Table 2. The EM-simulated and circuit modeled S-parameter results of the single via interconnection are shown in Fig. 4. As vertical interconnecting via is not an ideal coaxial line, the dispersion increase with the frequency increasing, which leads to non-linear distortion of transmission structure. Therefore, this non-linear distortion increases with frequency and length. From the corresponding results, it can be suggested that the developed circuit model and EM-simulation match almost well.

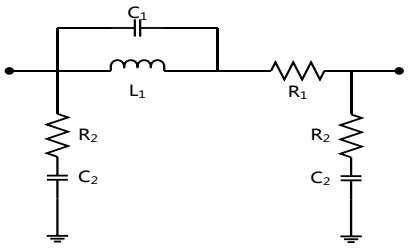


Fig. 3. Equivalent circuit for the proposed single vertical interconnection.

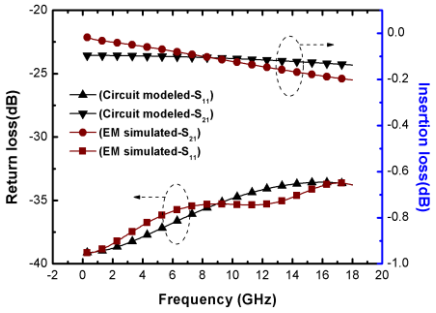


Fig. 4. EM-simulated and equivalent circuit modeled results of the proposed single vertical interconnection.

Table 2: Extracted model parameters

Lumped Parameters	Quantity	Data
C_1(fF)	Parasitic capacitance	85.86
C_2(fF)	Parasitic capacitance	22.38
L_1(pH)	Parasitic inductance	84.36
R_1(Ω)	Resistance	1.12
R_2(Ω)	Resistance	13.63

IV. MEASUREMENT

A back-to-back structure is manufactured for experimental validation as shown in Fig. 5. In Fig. 6, the measurement environment is displayed with a test fixture from Anritsu Model 3680V Universal. After firing, the average thickness of the LTCC substrate and the external conductor are 729 μm and 7 μm separately. The comparison of simulated and measured results has been shown in Fig. 7. For measurement results, the return loss is better than 10 dB, while the insertion loss is less than 1.59 dB in the frequency range of 0.3 GHz to 11.95 GHz. The simulation and measured results shows a discrepancy above 10 GHz. In practical manufacturing, due to fabrication tolerances, such as layer-to-layer alignment tolerance and dignment error of vertical via holes, the measured return loss (S11) of the fabricated model is less than the simulated result. In addition, due to mismachining tolerance of multi-metallized strips and the accuracy error of the shrinkage during the firing process, the measured insertion loss (S21) is larger than the simulated result. However, these factors are difficult to be considered in the simulation.

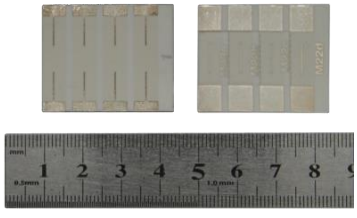


Fig. 5. Photographs of fabricated back-to-back interconnection modules (×4).

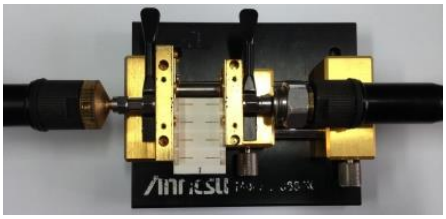


Fig. 6. Photograph of the testing environment.

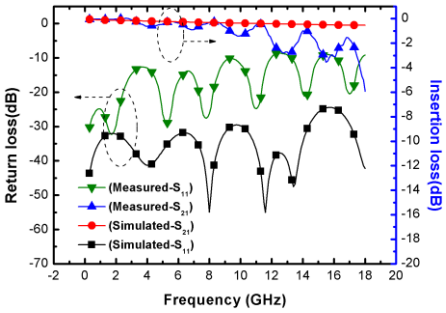


Fig. 7. Comparison of proposed study by simulated and measured results.

V. CONCLUSION

In this letter, a microwave microstrip-to-microstrip vertical via interconnect has been proposed and experimentally validated in LTCC technology. By using the coaxial-like signal via hole and the pad between microstrip and signal via hole, a better impedance matching and less discontinuity are achieved. Also, an improved equivalent circuit is developed for analyzing scattering characteristic of vertical via interconnects. The fabricated back-to-back structure shows an insertion loss of less than 1.59 dB and a return loss of better than 10 dB over 0.3 GHz to 11.95 GHz. This transition structure can be widely used in LTCC SiP module packaging applications.

ACKNOWLEDGMENT

This work was supported by Fundamental Science on EHF Laboratory of University of Electronic Science and Technology of China.

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