A CMOS Broadband Low-Noise Amplifier with Flat Gain Response for Ultra-Wideband Applications

Sen Wang and Wei-Han Yen
Department of Electronic Engineering, National Taipei University of Technology, Taipei 10608, Taiwan
e-mail : wangsen@ntut.edu.tw

***Abstract*—In this paper, a broadband distributed amplifier (DA) is presented. This circuit adopts the two-stage cascode gain cell and *m*-derived matching section to enhance gain and bandwidth performances. The series inductor placed at the inter-stage of the cascode cell can increase gain without any additional power consumption. A parallel resistor between the two-stage also enhances the gain flatness at low frequencies. The broadband DA is fabricated by a standard 0.18-µm CMOS process. The simulated results demonstrate that it achieves a gain of 10 dB, input and output return losses better than 8.3 and 8.56 dB, respectively. Isolation of this DA is better than 30 dB, and the noise figure is about 5.5 dB.**

Keywords—broadband amplifier; series inductor; CMOS.

I. INTRODUCTION

A DA is commonly applied to high-speed data links, satellite communications, high-resolution imaging systems, and ultra-wideband systems. Thanks to the distributed architecture, it provides such performance by absorbing the parasitic capacitances of parallel gain stages into an artificial transmission line, which not only results in the gain flatness and uniformity, but also lets input/output match within the bandwidth of operation [1]. Although conventional DAs can achieve a broadband bandwidth, its gain is not high due to the additive gain mechanism. In order to improve the gain of the DA, a cascade of inductively coupled common-source gain cells was proposed [2]. The DA uses a cascade gain cell to increase the gain and m-derive matching sections to reach input matching lower than –8 dB, and contains the gain 7.3±0.8 dB [3]. Besides, there are a lot of methods to improve the performance of DA. A CMOS DA with extended flat bandwidth and improved input matching by using gate lines and coupled inductors was be presented, and its input and output return losses are lower than 16 and 18 dB, respectively [4]. In [5-6], the DAs used four and five gain cells to achieve high gain and bandwidth flatness. In this paper, a two-stage cascode gain cell with a series inductor to extend the bandwidth, and the parallel resistor between two stages to enhance the gain flatness at low frequencies is presented.

II. CIRCUIT DESIGN

DAs can achieve broadband bandwidth because of the distributed architecture. A conventional DA in Fig. 1 consists of input and an output transmission lines coupled by the trans-conductance of the MOSFETs. The transmission lines are formed by using series inductors and gate-to-source capacitances of the transistors. In this topology, the input and output parasitic capacitances are absorbed in the distributed structures, which composed by these series inductors. Due to the distributed structure, the input and output signal can be not only separated obviously, but also enhance the isolation. The gain G of the conventional distributed amplifier has been analyzed in [2], by

$$G = \frac{n^2 g_m{}^2 Z_{0g} Z_{0d}}{4} \qquad (1)$$

where n is the number of the gain stages, g_m is the trans-conductance of each gain cell, and Z_{0g} and Z_{0d} are the characteristic impedance of input line and output line, respectively. From Equation (1), when the Z_{0g} and Z_{0d} are fixed to a certain value, the gain G of DA is affected by g_m and n. There is no limit on the number of stages in a DA with lossless artificial lines. However both gate and drain artificial lines are lossy in practice. Therefore, there is an optimum value for the number of stages, which is given by [4]. Although the gain can be increased by number of stages before it reaches a maximum number, the increasing stages results in larger die area and higher power consumption.

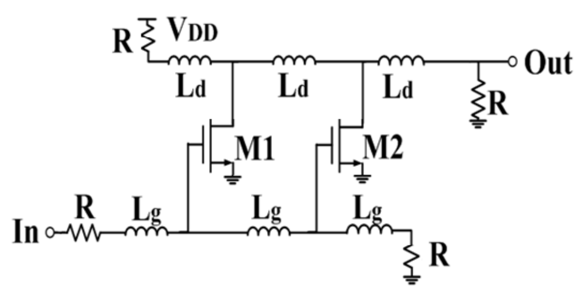

Fig. 1. A conventional distributed amplifier topology.

In this work, the CMOS DA was designed using two cascode gain cells, which provides high available gain, bandwidth and improves input-output isolation, and variable gain-control capability. As shown in Fig. 2, the DA uses *m*-derived sections to achieve the input matching network, and the series-peaking inductor (L_4) in gain cell extends the bandwidth without additional power consumption [4], and the parallel resistor between gain cells also enhances the gain flatness at low frequencies.

The simulation gain versus different parallel resistances is shown in Fig. 3. It is obvious that as the resistance becomes larger, and a flat gain response is achieved at low frequencies. In this work, 36 Ω is chosen for the resistance to obtain a flat gain response. The L_1, C_1 and C_2 (*m*-derived matching sections) are used to implement the input matching network. And the output matching network is designed by a buffer amplifier and L_3. The resistors R_b in the body of transistors $M_{1\text{-}4}$ are used to increase the overall gain in the circuit. The CMOS DA uses two stages to enhance the total gain with reasonable die area and small power consumption.

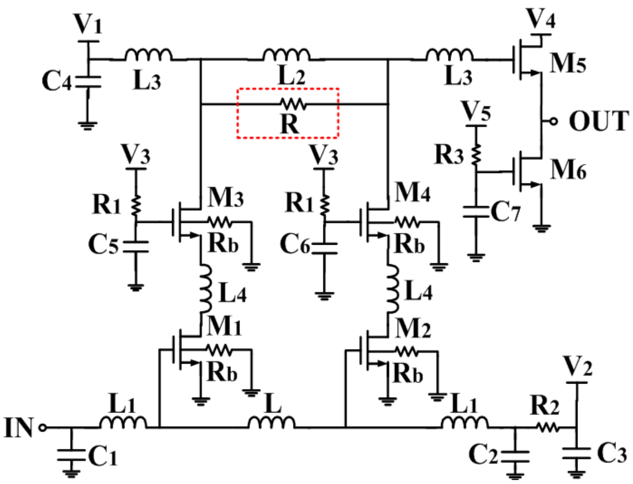

Fig. 2. Schematic of the proposed DA.

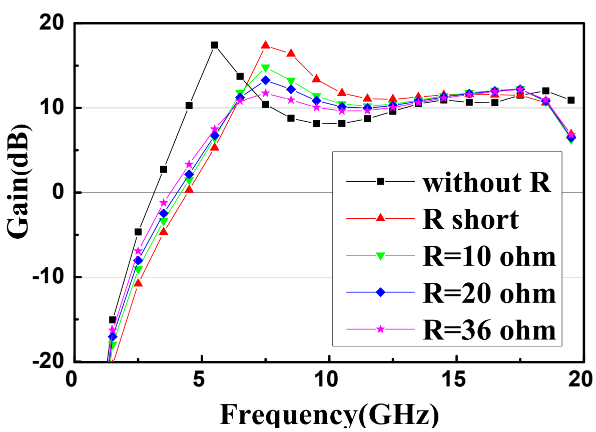

Fig. 3. Gain ($|S_{21}|$) simulation with different parallel resistors.

III. Discussion

The DA was designed using a 0.18-μm 1P6M CMOS process. The CMOS DA chip will be tested via on-wafer probing using ground-signal-ground air probes. At the bias conditions of V_1=1 V, V_2=0.78 V, V_3=1.5 V, V_4=0.85 V and V_5=0.8 V, the bias current of each gain cell and buffer of the DA was 5.95 mA and 3.76 mA. The resistance of R and R_b are chosen 36 Ω and 5 kΩ, which not only increase the total gain but also become flatness. Fig. 5 shows that the simulated power gain, the gain ($|S_{21}|$) is 10 dB with ripple 1 dB from 7 GHz to 19.5 GHz. The reverse isolation $|S_{12}|$ is -20 dB or better over the desired bandwidth. The input and output return losses are less than –8 dB in the entirely desired band. The noise figure is between 4.8 dB and 6.24 dB over the 7-19.5 GHz band, as shown in Fig. 5, and the chip area is 0.93×0.84 mm^2.

IV. Conclusion

A fully integrated broadband distributed amplifier has been designed, fabricated by using TSMC 0.18 μm CMOS process. The proposed amplifier consists of two-stage gain cell, which is a cascode-based topology to enhance the gain and bandwidth. In this circuit, the parallel resistance between two-stage is used to enhance the gain flatness at low frequencies, and the series inductor in one cell can extend the bandwidth without any additional power consumption. The simulation results show that the proposed DA is suitable for ultra-wideband communication applications.

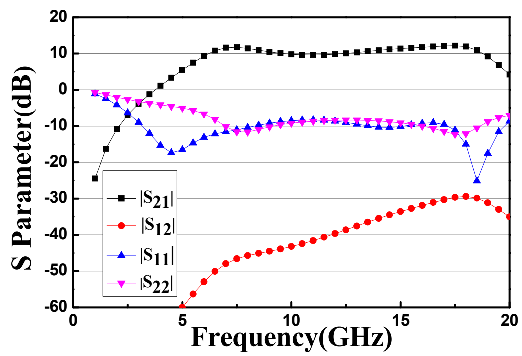

Fig. 4 The simulated *S* parameters.

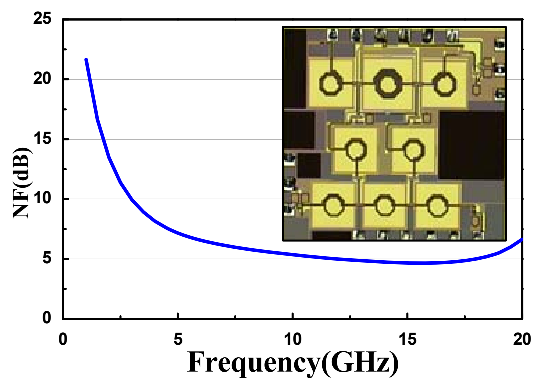

Fig. 5 Chip microphotograph and the NF.

References

[1] T. T. Y. Wong, *Foundamentals of Distributed Amplification*. Norwood, MA: Artech House, 1993.

[2] X. Guan and C. Nguyen, " Low-power-consumption and high-gain CMOS distributed amplifiers using cascade of inductively coupled common-source gain cells for UWB systems," *IEEE Trans. Microw Theory Tech*., vol. 54, no. 8, pp. 3278–3283, Aug. 2006.

[3] R.-C. Liu, K.-L. Deng, and H. Wang, "A 0.6–22-GHz broadband CMOS distributed amplifier," in *IEEE RFIC Symp. Dig*. June, 2003, pp. 103–106.

[4] K. Entesari, A. Tavakoli, and A. Helmy, " CMOS distributed amplifiers with extended flat bandwidth and improved input matching using gate line with coupled inductors," *IEEE Trans. Microw. Theory Tech*., vol. 57, no. 12, pp. 2862–2871, Dec. 2009.

[5] Ping Chen, Jui-Chih Kao, Pin-Cheng Huang and Huei Wang, " A Novel Distributed Amplifier with High Gain, Low Noise and High Output Power in 0.18-μm CMOS Technology , " *IEEE Microw. Symp. Dig*., June 2011.

[6] B. Y. Banyamin et al., "Analysis of the Performance of Four-Cascaded Single-Stage Distributed Amplifiers," *IEEE Trans. Microw. Theory and Tech*., vol. 48, no. 12, pp. 2657–2663, Dec., 2000.