# Modeling of CPW Based Passive Networks using Sonnet Simulations for High Efficiency Power Amplifier MMIC Design

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***Abstract*** – In this paper, the capabilities of the Sonnet software for accurate modeling and design of CPW based lumped-element resonators and matching networks is studied. A systematic method for design of complex matching networks using Sonnet is presented and good overall agreement between Sonnet simulations and measured s-parameter data from fabricated resonators and matching networks was obtained.

***Index Terms*** ─ CPW, EM simulation, GaN, high power, lumped element, matching network, MMIC, monolithic, passives, Sonnet.

## I. INTRODUCTION

High output power and high efficiency are two desirable factors for radio frequency (RF)/ microwave power amplifiers (PAs). Higher power added efficiency (PAE) leads to less DC power consumption by the circuit, therefore increasing the battery life and also relaxing the heat dissipation requirements. Monolithic microwave integrated circuits (MMICs) are of great interest in RF/Microwave application due to their much smaller size compared to the competing hybrid circuit technology. Among the existing microwave device technologies, AlGaN/GaN high electron mobility transistors (HEMTs) are particularly suitable for MMIC power amplifier applications due to their superior power-density and much higher breakdown voltage [1, 2, 3], and they have been successfully used in the past in MMIC power amplifier circuits [4,5].

Class B, C, and switch mode amplifiers such as Class E and Class F topologies are popular choices for high efficiency power amplifier applications. The issue of accurate input and output matching is especially important for these circuits since they are inherently narrow band tuned circuits and the gain, efficiency, and output power of the circuits are very sensitive to even minor mismatches in the matching networks and resonators. In order to obtain optimum circuit performance, it's essential to use accurate models for both the active HEMTs and the passive matching networks.

In this paper, the capabilities of the Sonnet software as an electromagnetic (EM) simulation tool for accurate modeling coplanar waveguide (CPW) based lumped element passive network is studied, and the results obtained from the simulations are compared against measured data from fabricated circuits. This particular topology was chosen because (i) due to lack of via technology in our fabrication process, we are limited to CPW environment for implementation of all passives and (ii) at lower microwave frequencies, lumped-element topology is the only feasible option for MMIC design due to the very large size of distributed elements at these frequencies. Nevertheless, the same design procedure could potentially be used for distributed structures and for microstrip environment.

This paper is not intended to compare the accuracy of Sonnet against other EM simulation software packages. The intention is simply to demonstrate the capabilities of the Sonnet software when it is used for a practical circuit design application, and the systematic design procedure that can be used for an accurate and efficient design for complex passive network.

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## II. FABRICATION

The lumped-element matching networks and resonators consist of parallel-plate capacitors and multi-turn spiral square inductors. The capacitors were fabricated using two 0.25 μm thick gold layers used for the parallel plates with a 130-nm thick SiN used for the dielectric layer. The dielectric constant of the SiN was experimentally determined to be about 7 at the RF/microwave frequencies of interest. A 3 μm gold layer was used for the ground planes and the interconnects.

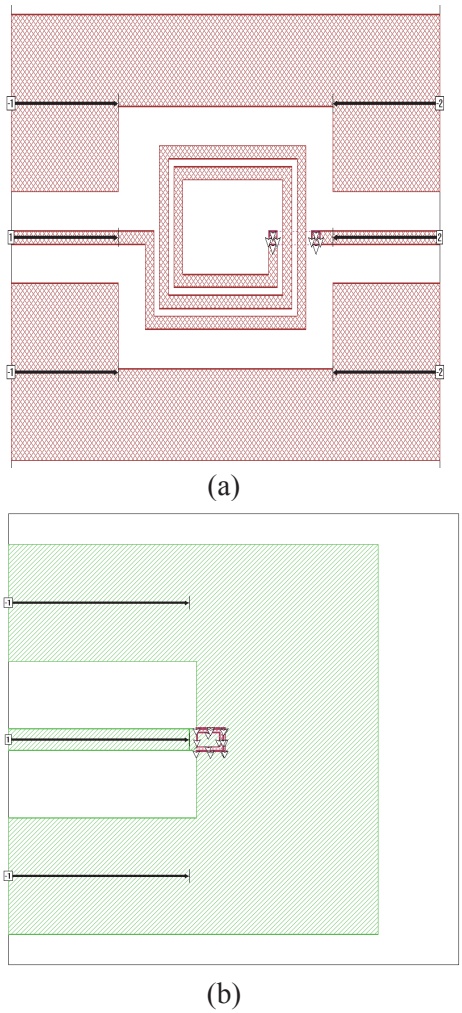
The multi-turn inductors were implemented using the 3 μm gold interconnect layer and a 1 μm gold bridge separated by a 3 μm bridge post made from PMGI SF-15 photoresis [6]. The PMGI may be etched away after fabrication to create a true air-bridge, but most often it is left in place considering its relatively large thickness and small dielectric constant. Process variations that most often affect the performance of the passive circuits include the thickness variation of the deposited SiN which affects the capacitance values and to a lesser extent the thickness variation of the deposited interconnect metal, which can affect the resistive losses. All circuits were fabricated at the UCSB Nanofabrication Facility.

## III. EM SIMULATION AND MODELING

There are a few approaches possible for designing passive networks. One approach relies on creating libraries based on measured s-parameters from fabricated inductors and capacitors of various sizes and geometries. In the absence of accurate EM simulation software, this is probably the most practical approach. However, this can be a very expensive and time consuming procedure since it requires fabrication and measurement of a large number of elements. Moreover, when the elements are placed in a circuit layout, it is difficult to accurately predict effects such as mutual coupling between the elements, the variations in the ground current paths (especially important in CPW environment) and the effects of all the interconnects using only these libraries.

Reliable EM simulation software can alleviate these problems mentioned above and allow for a much faster and more accurate way of modeling complex matching networks. The Sonnet software has proven to be a very accurate and powerful tool for planar EM simulations [7]. When the modeling is carried out in a systematic way, we will show that complex matching networks and resonators can be designed with excellent accuracy and minimum effort using Sonnet simulations.

Sonnet uses the method of moments applied directly to Maxwell's equations to solve planar problems. Detailed mathematical description of the method of moments and the theory used in Sonnet are found in [8] and [9], respectively, and an overview of Sonnet's operation can be found in [10]. This works quite well for modeling of passive networks used in MMICs because of their planar geometry.



(a) (b)

Fig. 1. (a) Layout of an inductor and (b) layout of a capacitor in Sonnet.

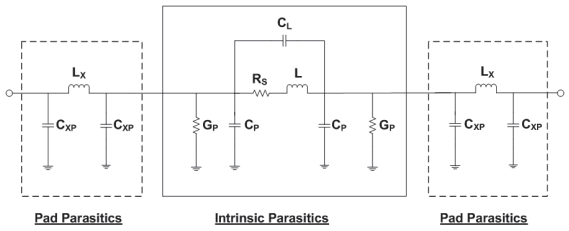
For accurate EM modeling it is important to simulate the elements exactly the same way that they are fabricated in the circuit. This will ensure

that the currents flow in the right directions and all fields are terminated correctly. Figure 1-(a) shows the layout of an inductor simulated in Sonnet. The inductor simulation consists of four dielectric layers: a 1000 μm glass plate where the substrate is mounted on ($\varepsilon_r$ = 3.9), a 300 μm sapphire substrate ($\varepsilon_r$ = 9.8, Loss Tan = 1.0 x $10^{-4}$), a 3 μm PMGI (1 <□$\varepsilon_r$ <2) bridge post, followed by a 3000 μm air column ($\varepsilon_r$ = 1) on the top. The dielectric constant of PMGI has negligible effect on the outcome of the simulations at the frequencies of interest and was fixed at $\varepsilon_r$ = 2. The metal layers consist of a 3 μm interconnect and a 1 μm bridge-metal gold layers. The metal type was set to NORMAL in the Sonnet simulator and a current ratio of 0.5 or larger resulted in the most accurate ohmic loss in the simulations.

The capacitors were similarly modeled with the glass plate and the sapphire substrate, followed by a 130 nm SiN dielectric layer ($\varepsilon_r$ = 7) between the capacitor plates, a 3 μm PMGI bridge post used for decreasing the parasitic capacitance due to the interconnect metal, and a 3000 μm air column on the top. All connections between the metal layers were made using vias through the dielectric layers. Figure 1-(b) shows the layout of a capacitor simulated in Sonnet.

## IV. PASSIVE NETWORK SIMULATION AND MODELING

Initially, inductors of various sizes and geometries were simulated in Sonnet, and a high frequency equivalent circuit model was extracted from each simulation in order to create a simulation based inductor library. Figure 2-(a) shows the high frequency equivalent circuit model used for the inductors. The intrinsic section of the model consists of a pie network. The series resistor models the conductor loss in the metal, and the shunt resistors account for the loss in the substrate. All resistor models consist of a frequency dependent component that accounts for high frequency losses. The shunt capacitors are used to model the parasitic capacitance between the inductor and ground. These capacitors are the main factors in determining the inductor's self resonance. The capacitor parallel with the inductor is used for modeling the capacitance between the inductor's loops and its value is usually negligible. The pad parasitic elements are not needed for model extraction from the Sonnet simulations since Sonnet allows de-embedding up to the inductors terminals, and their corresponding values should be set to zero. They are only used for model extraction from measured data (test structures), in which case they need to be extracted separately using open and short pad structures prior to the intrinsic model extraction. Figure 2-(b) shows the extracted equivalent circuit vs. Sonnet simulation results for an inductor. The inductor used in this simulation has n = 2.5 turns, line thickness of 50 μm, line separation 30 μm, ground plane width of 300 μm, and ground plane separation of 150 μm.

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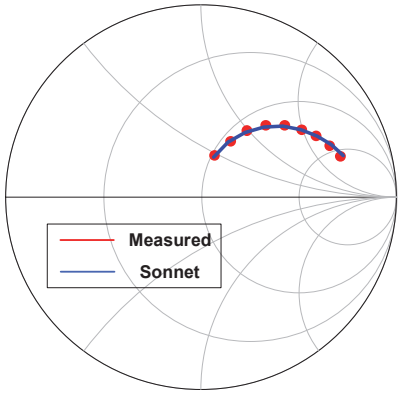
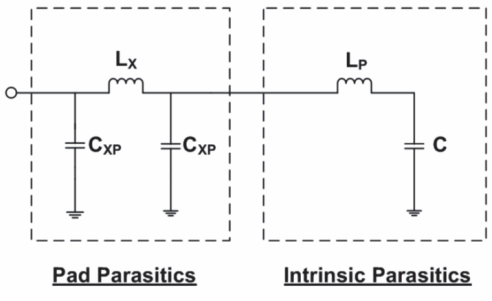



(b)

Fig. 2. (a) High frequency equivalent circuit model and (b) Sonnet simulation vs. extracted equivalent circuit model for an inductor.

The capacitor modeling and parameter extraction procedure is similar to that of inductors. Since our designed matching networks required only shunt capacitors, the capacitor simulations were carried out as one-terminal simulations with capacitors terminating in the ground plane. Figure 3-(a) shows the high frequency circuit model used for modeling capacitors in ADS. The model consists of the capacitor in series with a parasitic

inductor. Due to the small size of the capacitors, the value of the series inductor is normally very small. The capacitance values scale quite well with geometry, and hence the creation of a capacitor library was unnecessary. Figure 3-(b) shows the extracted high frequency equivalent circuit vs. Sonnet simulation results for a capacitor.

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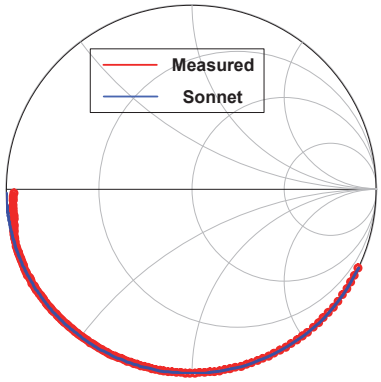
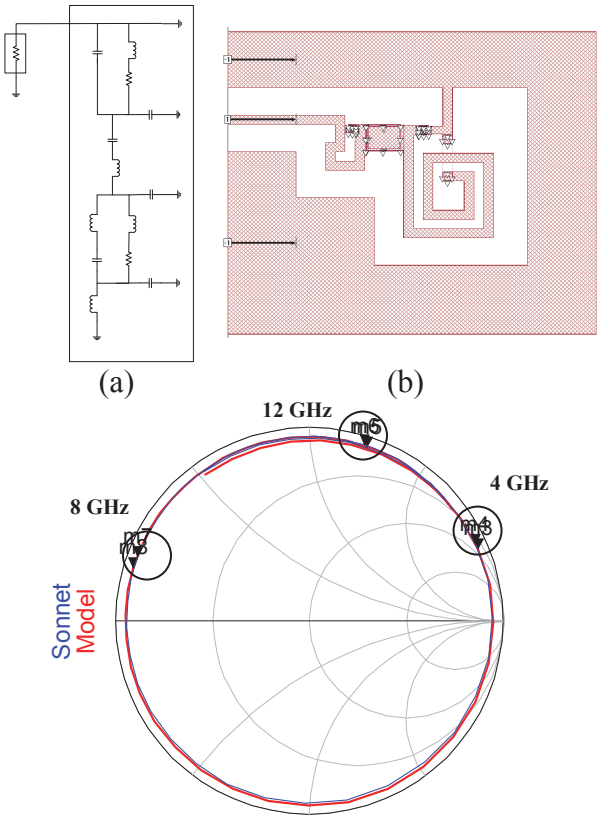



(b)

Fig. 3. (a) High frequency equivalent circuit model and (b) Sonnet simulation vs. extracted equivalent circuit model for a capacitor.

All parameter extractions were carried out in Agilent's advanced design systems (ADS) [11] with the aid of optimization routines. However, in general any other circuit simulation software capable of performing s-parameter simulations and basic optimization can be used to perform the parameter extractions for the equivalent circuits. The optimization routine used for the majority of the model extractions was the gradient method. However, the Quasi-Newton, least p-th, and hybrid routines also resulted in a good fit.

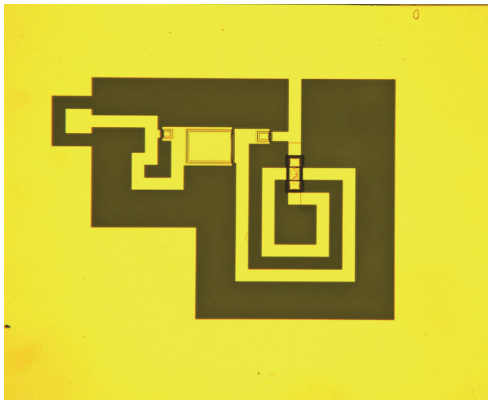



(a) (b) (c)

Fig. 4. (a) High frequency equivalent circuit, (b) Sonnet layout, and (c) Sonnet vs. circuit model s-parameter simulation results for the resonator.

## V. MATCHING NETWORKS RESULT

In this section, the design of two output networks for a class F MMIC power amplifier is discussed. These relatively complex circuits serve as good examples for demonstrating the capabilities of Sonnet in correctly simulating their performance. The details of the class F amplifier operation are beyond the scope of this paper and here we will suffice in examining the performance of the designed output networks. The first output network consists of an L matching network and a resonator. The matching network and the resonator were initially designed separately, and then combined and optimized to obtain the complete output network. The optimization steps are needed to compensate for effects such as the changing of the current paths in the ground planes, the coupling between different components and the added interconnects when discrete lumped elements are combined together.



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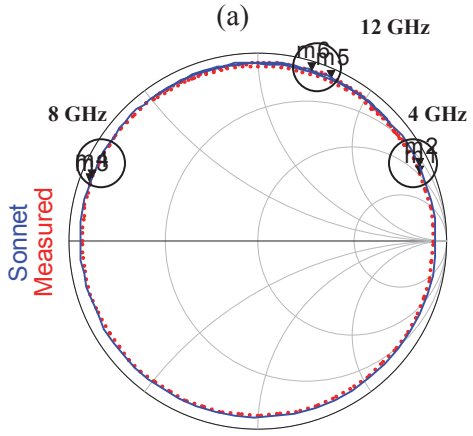
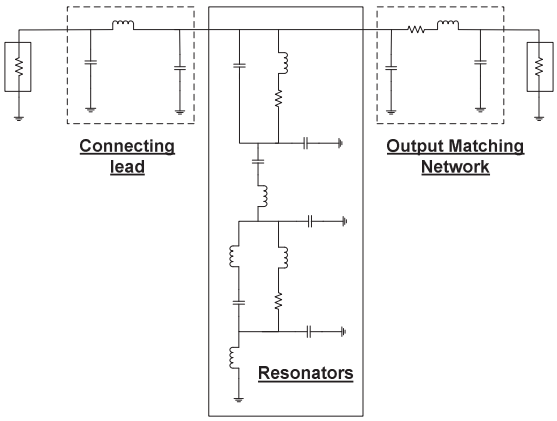



(b)

Fig. 5. (a) The fabricated resonator (b) Sonnet simulation vs. measured s-parameter results for the designed resonator.

Each section was initially designed in ADS using the equivalent circuit models for the inductors and capacitors, taking into the account all the parasitic elements. The layout of the designed networks were then simulated and optimized in Sonnet by adjusting the size and geometry of the capacitors and inductors as needed. Figure 4 shows the equivalent circuit model vs. Sonnet simulation s-parameter response obtained for the resonator circuit alone. We can see that excellent match is obtained over a wide frequency range. The fabricated resonator test structure is shown in fig. 5-(a), and the measured s-parameter result vs. the Sonnet simulation is shown in fig. 5-(b). We can see that excellent match is obtained between the measured data and the Sonnet simulation.

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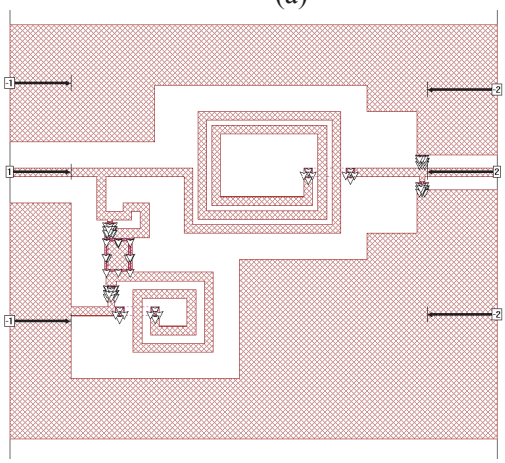

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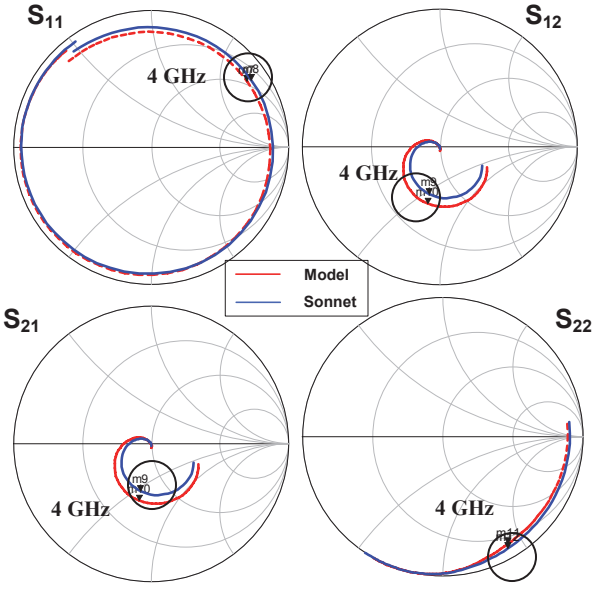


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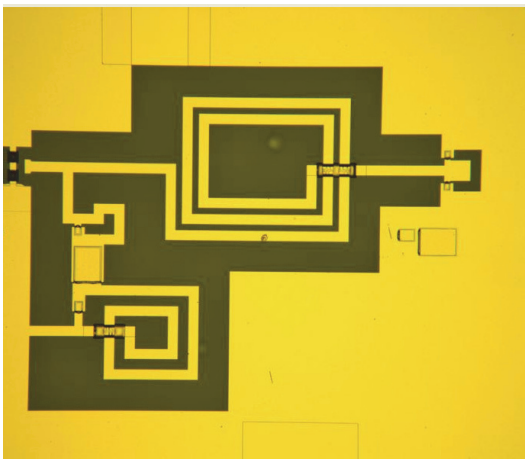
Fig. 6. (a) High frequency equivalent circuit, (b) Sonnet layout, and (c) Sonnet vs. circuit model s-parameter simulation results for the first output network.



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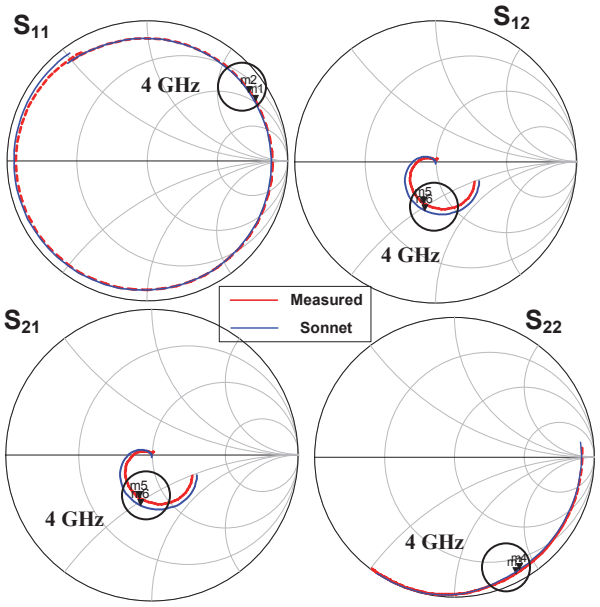
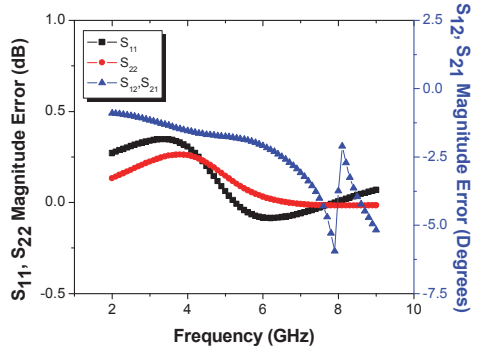



(b)

Fig. 7. (a) The fabricated output matching network (b) Sonnet simulation vs. measured s-parameter results for the first output network.

Finally, the two sections were combined to form the complete output network and final optimizations were carried out. At this point, the circuit becomes quite large and the simulations can take up a lot of time. However, due to the previous optimization of the individual sections the final optimization should not take much iteration. Figure 6 shows the equivalent circuit model vs. Sonnet simulation for the complete output matching network and fig. 7 shows the Sonnet simulation vs. measured results obtained from the fabricated circuit. From the two figures,

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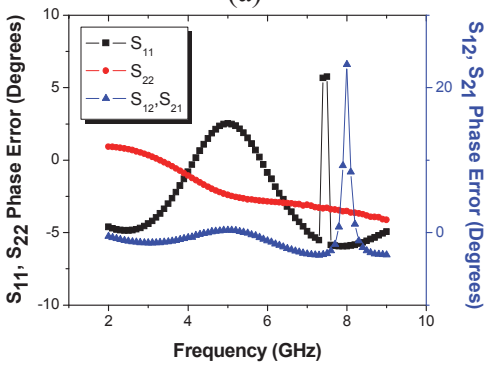


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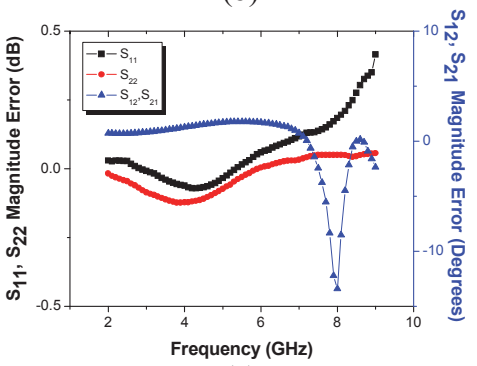


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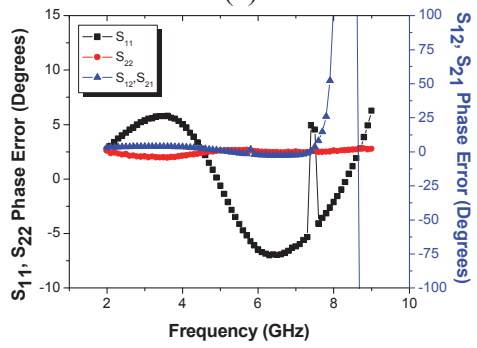



(d)

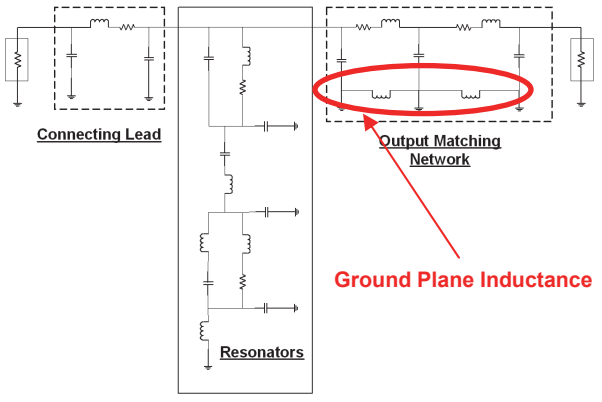
Fig. 8. Error plots of (a) magnitude and (b) phase of the equivalent circuit model vs. Sonnet simulation and (c) magnitude and (d) phase of measured data vs. Sonnet simulation for the first output network.

we can see that good overall fit is observed between the equivalent model simulation, the Sonnet simulation, and the measured data.

In order to better see the extent of agreement between the equivalent circuit model, Sonnet simulation, and measured data, the amplitude and phase errors are plotted in fig. 8. We can see that in both cases, $S_{11}$ and $S_{22}$ magnitude errors are less than ±0.5 dB and the phase errors are mostly within ±5 degrees. The $S_{12}$ errors are small at lower frequencies. However, at higher frequencies as the magnitude of the $S_{12}$ decreases rapidly, the magnitude and phase errors start to increase substantially. At such small values of $S_{12}$ however, these errors have a negligible effect on the performance of the circuit.

The second output network consists of a π matching network and the same resonator structure at the drain side. Figure 9-(a) shows the equivalent circuit model and fig. 9-(b) shows the Sonnet layout of this output network. It can be seen from the layout that this output network is quite more complex compared to the previous example. Initially, there was a significant mismatch between the response of the equivalent circuit model and the Sonnet simulated s-parameters. After some analysis, it was determined that the mismatch is caused by the large asymmetry in the shape of ground planes on the layout, which has a substantial effect on the ground currents. This effect can be modeled in the equivalent circuit model by addition of small amounts of parasitic inductance in the ground paths, as marked on figure 9-(a). When these parasitic inductances were added to the equivalent circuit model, much improved match between the model and the Sonnet simulations was obtained, as shown in figure 9-(c). Figure 10 shows a picture of the fabricated output network and the comparison between the Sonnet simulations and the measured s-parameter response. We can see that good overall match between the Sonnet simulations and the measured data is obtained here as well.

Figure 11 shows the magnitude and phase error plots for the second output circuit. We can see that for this circuit, $S_{11}$ and $S_{22}$ magnitude errors are within ±1 dB and the phase errors vary from -5 to +25 degrees. These errors are notably larger than the errors seen in the previous circuit, reflecting the increased complexity of this circuit compared to the first circuit.

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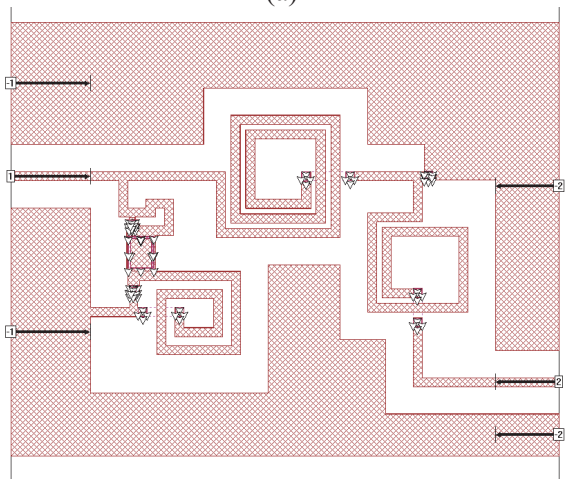

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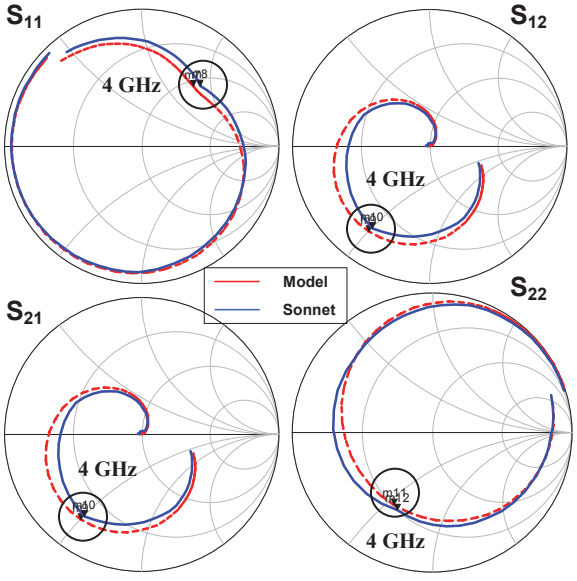
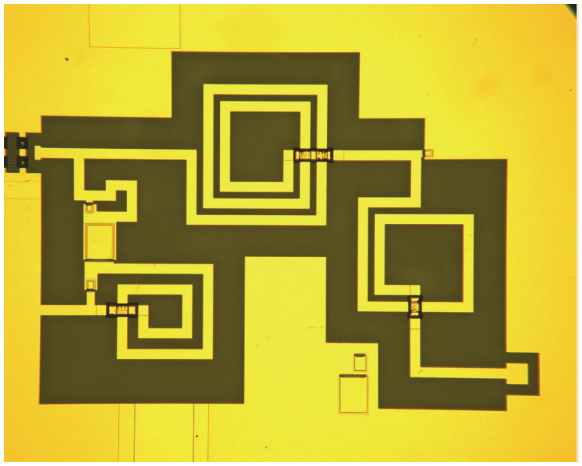



(c)

Fig. 9. (a) High frequency equivalent circuit, (b) Sonnet layout, and (c) Sonnet vs. circuit model s-parameter simulation results for the second output network.



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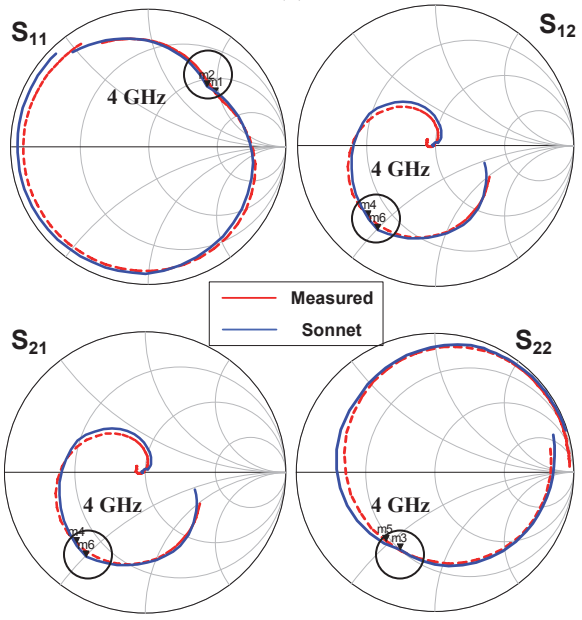
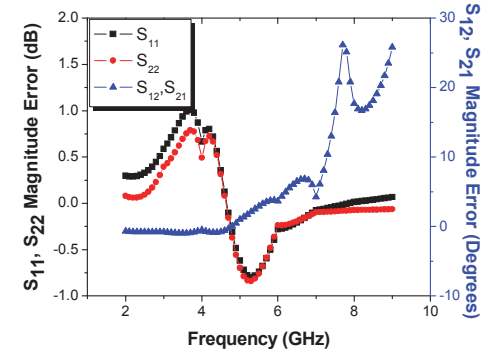



(b)

Fig. 10. (a) The fabricated output matching network and (b) Sonnet simulation vs. measured s-parameter results for the second output network.

The $S_{12}$ errors are comparable to those of $S_{11}$ and $S_{22}$ at lower frequencies. Again at higher frequencies as the magnitude of $S_{12}$ starts to decrease rapidly, the magnitude and phase errors increase substantially, but the effect of these errors are negligible on the performance of the circuit at such small values of $S_{12}$.

All simulations were performed on a Dell Precision 380 desktop containing a dual core 3.00 GHz Pentium D microprocessor and 3.5 GB of RAM. For all circuit simulations in Sonnet, the cell size was set to 2 μm in both X and Y directions, and the simulations were performed

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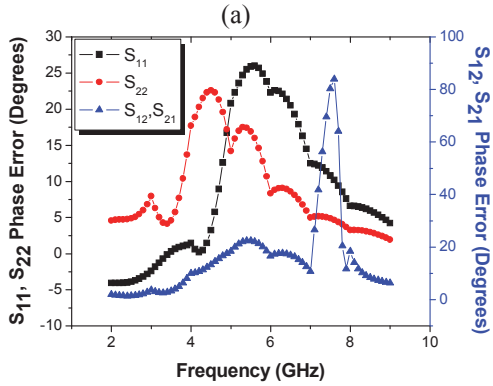


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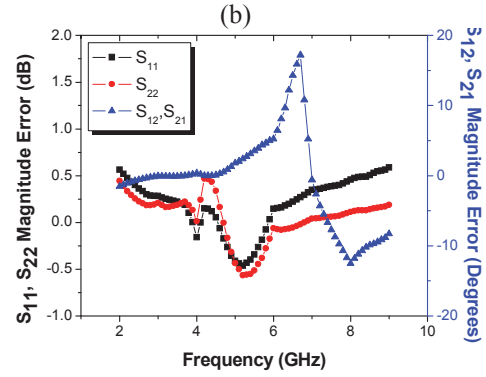


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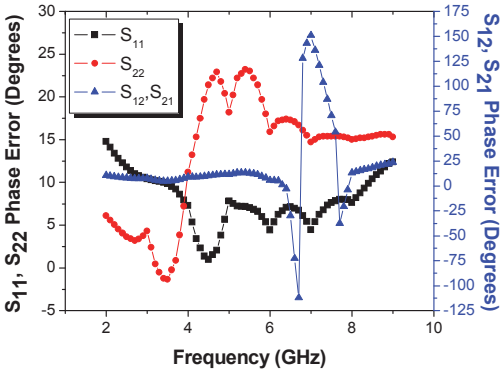


(d)

Fig. 11. Error plots of (a) magnitude and (b) phase of the equivalent circuit model vs. Sonnet simulation and (c) magnitude and (d) phase of measured data vs. Sonnet simulation for the first output network.

from 1 GHz to 16 GHz using the adaptive sweep (ABS) option. The resonator circuit layout shown in figure 4 has a box size of 2200 μm x 2200 μm in the Sonnet simulation window. The simulation time for this circuit was 101 minutes and 9 seconds. For the first output network shown in fig. 6, the final box size in the Sonnet simulation window was 2800 μm x 3000 μm and its simulation time was 224 minutes and 35 seconds. The second output network shown in fig. 9 has a box size of 3000 μm x 3000 μm and the simulation time for this circuit was 218 minutes and 42 seconds.

## VII. CONCLUSION

Accurate modeling of CPW based passive components and design of matching networks using Sonnet was discussed in this paper. Initially, individual inductors and capacitors of various sizes and geometries were simulated in Sonnet, and a high frequency circuit model was extracted from each components. These extracted results were used to create a simulation-based inductor library and a scalable capacitor model, which were then used in designing complex passive circuits including resonators and matching networks. The systematic approach used for the design of complex passive networks resulted in obtaining accurate results with reduced time and effort spent. Based on these results Sonnet proved to be a powerful tool for accurate design of complex passive circuits.

## ACKNOWLEDGMENT

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