Coplanar Waveguide Slot-coupled K_a-band Patch Antenna for Integration with Wafer-scale Beam-steering MEMS Control Board

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Abstract – A coplanar waveguide (CPW) slot-coupled K_a-band patch antenna is designed, constructed and tested for subsequent integration with a wafer-scale MEMS-switched antenna array beam-steering control board. The antenna is designed for fabrication on a high resistivity silicon (HRS) wafer ($\varepsilon_r \approx 11.8$) for operation with 25-30 GHz satellite communication systems. A simulated 10 dB return loss bandwidth of 2.96 GHz (9.8 %) is achieved with a 4.6 dB peak gain and 110° half-power beamwidth (HPBW). A scaled prototype at 6 GHz is constructed on RT/Duroid 6010 substrate ($\varepsilon_r \approx 10.2$) and yields a measured bandwidth of 360 MHz (6.0 %) and a peak gain of 4 dB. A CPW feedline / slot misalignment sensitivity test is conducted through simulations to investigate the effects that fabrication errors may have on antenna performance during wafer-scale integration of the patch antenna onto the HRS substrate. Simulation results show that slot misalignment less than 200-400 μm should only minimally affect antenna performance, with the most significant degradation being a 2.5 – 4.0 % drop in antenna bandwidth. The successful design of this patch antenna demonstrates a compact, efficient method for integration of a CPW slot-coupled K_a-band patch antenna onto a wafer-scale MEMS control board without the need for additional substrate layers or feedline interconnects, minimizing total system weight and fabrication complexity.

Keywords: Coplanar waveguide, patch antenna, wafer-scale, and MEMS.

I. INTRODUCTION

Several key metrics including size, efficiency, and affordability must be optimized when Army communication systems are designed. With this in mind, research on embodiments of a compact, efficient microwave electronic scanning array (ESA) has been proposed for integration with future battlefield platforms. One such ESA involves a K_a-band aperture-coupled patch antenna array as the radiating element on a wafer-scale MEMS-switched control board for a lightweight, compact electronically-controlled beam and null steering unit for satellite communication systems. Integration of a patch antenna array onto such a wafer-scale control board requires a design approach that differs from the traditional aperture-coupled microstrip patch antenna technique, since the feedlines that extend from the MEMS switching elements are typically coplanar waveguide (CPW) structures. The design, simulation and testing of a single K_a-band patch antenna will be discussed, with a focus on its future integration with a CPW-fed wafer-scale MEMS-switched control board.

II. DESIGN APPROACH

The first step in the design of a K_a-band patch antenna for integration with a wafer-scale MEMS control board is to develop a solid understanding of the wafer structure and the MEMS-switched beam/null-steering control board design. The MEMS switches are fabricated onto a 4" diameter, 500 μm thick high resistivity silicon (HRS) wafer ($\varepsilon_r \approx 11.8$, $\tan(\delta) \approx 0.02$, $\sigma < 0.01$ S/m) with gold trace used for the transmission lines and the ground plane. While microstrip feed lines are typically used for aperture-coupled patch antennas, CPW transmission lines are most easily fabricated on the HRS wafer where the MEMS switching elements reside. While research on this topic has been scarce, especially prior to the early 1990s, the recent interest in incorporating active antennas into monolithic microwave integrated circuits (MMICs) has yielded a number of papers that detail promising techniques for CPW aperture coupling. One such technique involves two substrates, with the CPW line on the lower surface of the bottom substrate. A ground plane with an aperture is placed on the upper surface of this substrate and a second substrate is placed on top of this structure, with a patch antenna located on its upper surface. The CPW line couples energy through the aperture to the patch antenna similar to the traditional microstrip aperture coupling approach [1-3]. Another technique involves a single substrate and completely eliminates the need for an embedded aperture and ground plane between two separate substrates [4, 5]. With this

technique, a patch antenna is fabricated on the upper surface of a substrate and a CPW feedline is fabricated on the lower surface, with a coupling slot integrated beneath the patch at the end of this feedline. The CPW feedline couples energy directly through this slot to the patch. One recent embodiment of this approach incorporated a novel tuning stub into the CPW feedline for important reactive tuning for better impedance matching [5].

The integration of a K_a-band patch antenna with a CPW-fed MEMS control board required careful consideration of fabrication ease and substrate dimension constraints. A center frequency of ~30 GHz was chosen in order to facilitate the usage of a final wafer-scale MEMS-switched antenna array based on this design as the uplink mechanism for a typical satellite communication system. At 30 GHz, the 500 µm HRS substrate tended to be too thick to serve as the lower substrate in a two-substrate aperture-coupling setup. Test simulations in HFSS yielded a much higher bandwidth of ~6-7% using the single-substrate CPW aperture-coupling method [4, 5] than the ~1-2% bandwidth yielded by the two-substrate method [1-3]. In addition to this notable bandwidth improvement, the single-substrate technique also reduces fabrication complexity by incorporating the control board and antenna on the same structure and reduces the weight of the final unit by eliminating the need for additional substrate layers to be bonded to the HRS wafer. Thus, the single-substrate CPW slot-coupling method was chosen for the final 30 GHz patch antenna design, with the tuning stub pioneered in [5] included for reactive tuning.

III. WAFER-SCALE PATCH ANTENNA DESIGN/SIMULATION

A CPW slot-coupled patch antenna was then designed from patch antenna and coplanar waveguide theory [6, 7] and was simulated and fine-tuned in *Ansoft* HFSS [8] and *EMAG* EMPiCASSO [9], with the CPW feedline incorporated into the ground plane of the HRS substrate and a tuning stub included for reactive impedance matching. The final antenna design is shown in Fig. 1, with detailed dimensions and substrate properties listed in Table 1.

The simulated return loss for this CPW slot-coupled patch antenna design is shown in Fig. 2. In HFSS, an excellent resonance at ~30.2 GHz was obtained after the patch antenna dimensions and CPW feedline characteristics were fine-tuned accordingly from theoretical values to their final values listed in Table 1, with a resulting 10 dB return loss bandwidth of ~2.96 GHz (9.8 %), from 28.59 – 31.55 GHz. The EMPiCASSO return loss results exhibit a center frequency shift up to ~30.5 GHz and a 10 dB return loss bandwidth decreases down to ~1.62 GHz (5.3 %), from 29.69 – 31.31 GHz. The causes of these small discrepancies between the HFSS and EMPiCASSO results will be discussed when the measured data for a scaled prototype is presented.

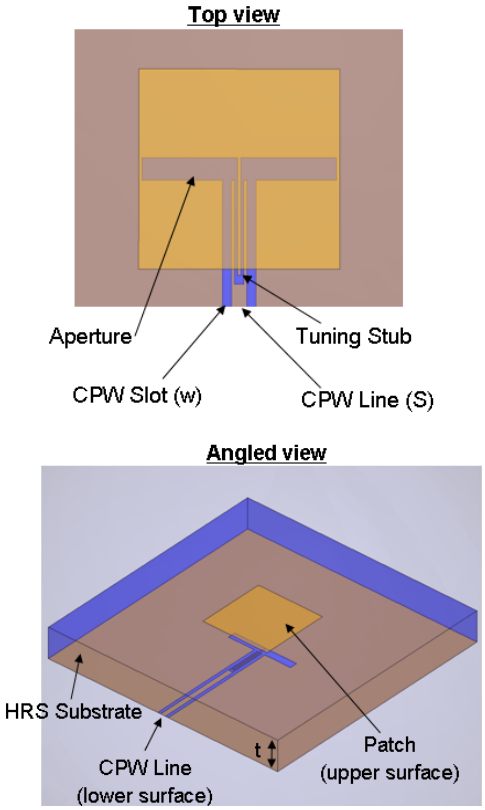

Fig. 1. HFSS model of a 30 GHz CPW slot-coupled patch antenna.

Table 1. 30 GHz CPW slot-coupled patch antenna design parameters.

Variable	Dimensions
Patch	1115 x 1115 µm
Substrate	4000 x 4000 µm, t = 500 µm
CPW line width (S)	85 µm
CPW slot width (w)	50 µm
Slot dimensions	1078 x 124 µm
Tuning stub length (from bottom edge of aperture)	530 µm
Substrate material properties	$\varepsilon_r \approx 11.8$, $\tan(\delta) \approx 0.015$, $\sigma <$ 0.01 S/m
Patch / CPW feedline material properties	Gold trace: $\sigma \approx 4.7e07$ S/m, t = 0.75 µm

The simulated gain for this antenna design is shown in Fig. 3. The peak gain occurs at 0° and is ~4 dB, with a half-power beamwidth (HPBW) of ~110°. The low gain value is mainly attributed to the lossy HRS wafer that the antenna resides upon, with a high dielectric constant, relatively large thickness, and low resistivity compared to most low-loss substrates used for traditional patch antenna designs. This reduction in gain has been deemed a fair tradeoff for the ease of fabrication and unit weight reduction that results from the single-substrate integration of the antenna directly onto the HRS wafer.

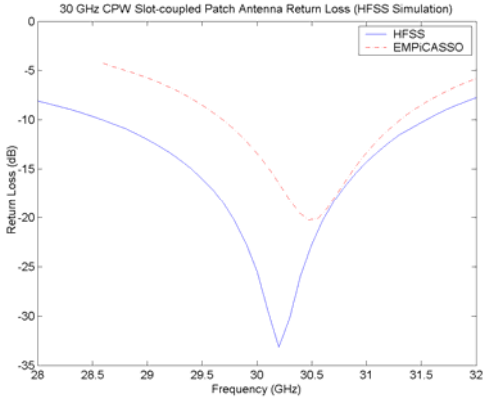

Fig. 2. HFSS-simulated S_{11} data for 30 GHz CPW slot-coupled patch antenna.

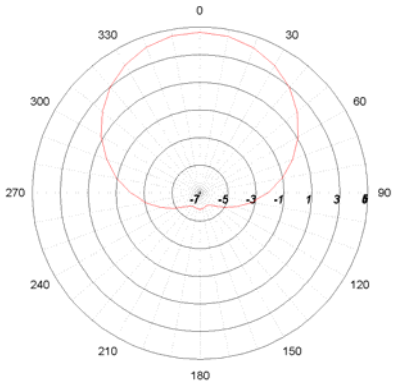

Fig. 3. HFSS-simulated total gain pattern for 30 GHz CPW slot-coupled patch antenna.

IV. SCALED PROTOTYPE ANTENNA SIMULATION/MEASUREMENTS

Since this design was too small to be constructed with an on-site router (6 mil bit size limitation), the antenna frequency was scaled down to 6 GHz in order to increase the structure size enough so that a test unit could be efficiently and accurately fabricated. Detailed dimensions and substrate properties are summarized in Table 2. A single element prototype of this 6 GHz design was then constructed on a 3" x 3", 2.54 mm thick RT/Duroid 6010 substrate ($\varepsilon_r \approx 10.2$) with an end-launch coaxial cable connector soldered to the CPW line. RT/Duroid 6010 substrate was used in place of the HRS wafer due to its reasonably similar dielectric constant, ε_r. A picture of this prototype is shown in Fig. 4. The return loss data for this prototype is shown in Fig. 5.

Table 2. Scaled prototype CPW slot-coupled patch antenna design parameters.

Variable	Dimensions
Patch	5.67 x 5.67 mm
Substrate	76.2 x 76.2 mm, t = 2.54 mm
CPW line width (S)	0.91 mm
CPW slot width (w)	0.41 mm
Slot dimensions	5.45 x 0.57 mm
Tuning stub length (from bottom edge of aperture)	3.25 mm
Substrate dielectric constant	$\varepsilon_r \approx 10.2$

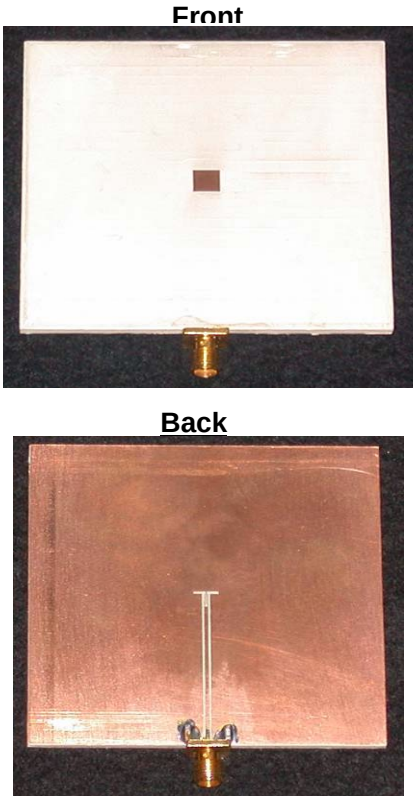

Fig. 4. Fully-constructed 6 GHz scaled prototype of CPW slot-coupled patch antenna.

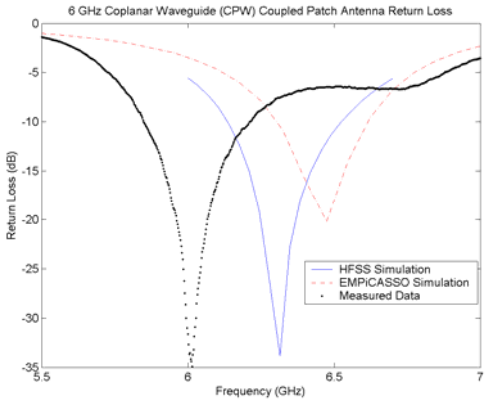

Fig. 5. Measured S_{11} data for 6 GHz prototype CPW slot-coupled patch antenna.

While the measured return loss for this 6 GHz prototype ended up having a center frequency about ~300-500 MHz lower than the HFSS and EMPiCASSO results, it did confirm the feasibility of the excellent HFSS simulation results of the 30 GHz design. A resonance at ~6.01 GHz was obtained with a 10 dB return loss bandwidth of ~360 MHz (6.0 %), from 5.85 – 6.21 GHz. This measured bandwidth is nearly double the achieved bandwidth of existing single-substrate CPW-fed slot-coupled patch antenna designs [4], [5]. E-plane and H-plane radiation pattern measurements are shown in Figs. 6 and 7.

The resulting peak gain for this prototype was 4.4 dB. While a generally broadside radiation pattern is confirmed by these measurements, a small drop of 1-2 dB is seen in the E-plane radiation pattern between -10° and 15°. HFSS simulation results for the 6 GHz scaled patch antenna with a 3" x 3" substrate, also shown in Figs. 6 and 7, confirms this phenomenon and matches the measured data reasonably well in shape and final realized gain.

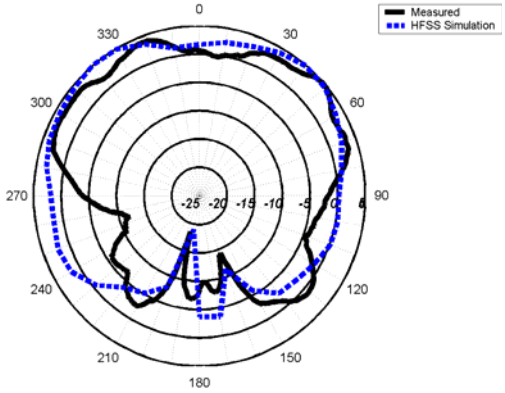

Fig. 6. Measured E-plane radiation pattern data for 6 GHz prototype CPW slot-coupled patch antenna.

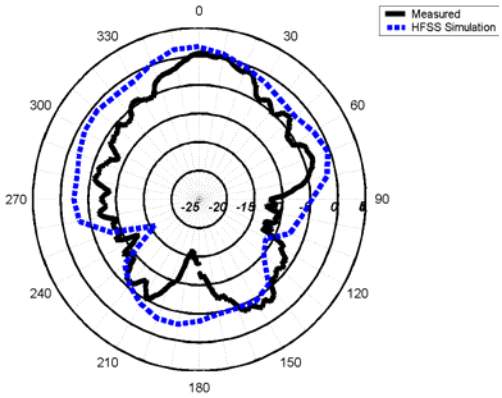

Fig. 7. Measured H-plane radiation pattern data for 6 GHz prototype CPW slot-coupled patch antenna.

The 0° dip in the measured prototype results is a significant deviation from the simulated 30 GHz wafer-scale patch antenna total gain pattern shown in Fig. 3. This simulated patch antenna was placed onto a substrate that was approximately 4 times larger in size than the patch area. The scaled 6 GHz prototype, however, was constructed on a substrate that was 15 times larger than the patch antenna. Increased surface wave radiation from this notable increase in substrate / ground plane size is expected to be the cause of the measured radiation pattern abnormalities. In order to confirm this theory, HFSS simulations were conducted with the 6 GHz scaled prototype design placed on substrates of different sizes. The resulting E-plane and H-plane radiation patterns are shown in Fig. 8 and 9. A slight tilt towards 5° exists in the broadside E-plane pattern maximum with the 1-inch substrate, but the 0° power loss is significantly mitigated. The general trend observed from comparing this simulation data is that the overall radiation pattern tends to become a more efficient broadside pattern as the substrate size is decreased. Considering that surface wave contributions to patch antenna radiation increase as the substrate size increases, particularly in the E-plane [10], these results strongly indicate that surface wave diffraction from the substrate edges are the main cause of the slightly-degraded radiation pattern [10-12]. The final wafer-scale patch antenna array will be incorporated onto a silicon wafer approximately 100 times larger (4" x 4") than an individual patch antenna, so techniques for mitigating the effect that this surface wave diffraction has on the final antenna array gain and radiation pattern should be explored further. A promising candidate for reducing this surface wave distortion is the incorporation of an electromagnetic bandgap (EBG) structure [10, 13] or a uniplanar compact photonic bandgap structure (UC-PBG) [14, 15] onto the silicon wafer. The next phase of research for this wafer-scale patch antenna array will focus on the incorporation of such a structure into this design for further optimization of the antenna radiation performance.

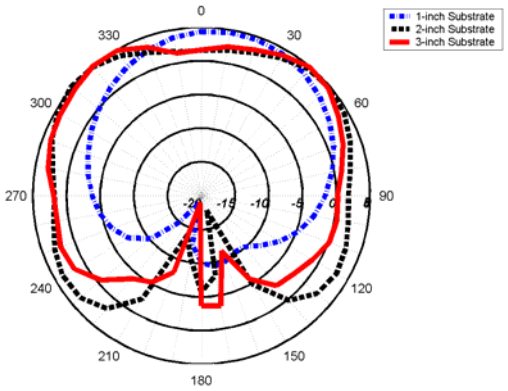

Fig. 8. Effect of substrate/ground plane size on E-plane radiation pattern for 30 GHz wafer-scale patch antenna.

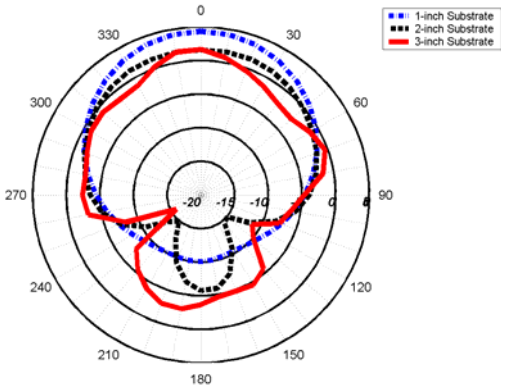

Fig. 9. Effect of substrate/ground plane size on H-plane radiation pattern for 30 GHz wafer-scale patch antenna.

A comparison of the HFSS and EMPiCASSO simulated return loss plots in Fig. 2 and 5 yields a consistent relationship between the two simulation program results for both the 30 GHz wafer-scale design and the 6 GHz scaled prototype design. In both cases, the EMPiCASSO results show less-pronounced resonance at a center frequency about 150 – 200 MHz higher than the HFSS results and exhibits a 2 – 4 % bandwidth decrease. When placed side-by-side with the 6 GHz measured data, the HFSS simulation results are much closer than the EMPiCASSO simulation data, yielding a very similar resonance shape and bandwidth and only having a +300 MHz center frequency shift versus the less comparable resonance shape and +475 MHz shift that the EMPiCASSO results displayed. The less accurate results obtained by EMPiCASSO are likely attributed to its 2.5D geometry scheme which employs an infinite substrate and ground plane size. The > 300 MHz difference between the simulated and measured results for this prototype could also be attributed to fabrication/measurements inaccuracies and to limitations in the simulation model. Even with these small discrepancies between simulated and measured results, the data obtained from the 6 GHz scaled prototype demonstrate the effectiveness that the 30 GHz wafer-scale design should have when it is fabricated onto an HRS substrate.

V. WAFER-SCALE FABRICATION ERROR SENSITIVITY TEST

When this patch antenna design is fabricated onto an HRS wafer, there is a potential for misalignment between the patch on the upper surface of the wafer and the CPW feedline and slot on the lower surface. Using a photoetching process, this misalignment should be limited to a worst-case offset of ~5 µm. An alignment sensitivity test was conducted in HFSS to predict what effects this misalignment would have on the patch antenna performance. The CPW feedline and slot were both offset from their centered position under the patch antenna by 5 µm along the x-plane and then the y-plane. A diagram of this feedline/slot offsetting strategy is shown in Fig. 10.

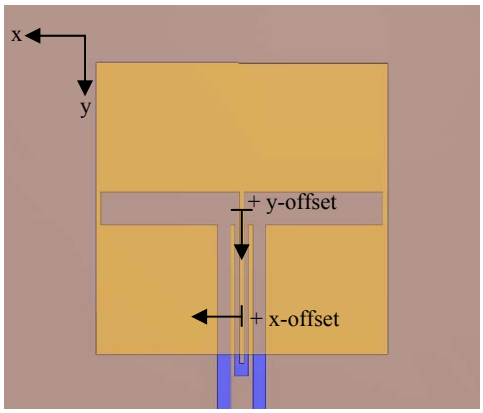

Fig. 10. Offset orientation diagram for CPW feedline / slot alignment sensitivity test.

A comparison of the HFSS-simulated returns loss for these misaligned cases with that of the perfectly-aligned case is shown in Fig. 11. The +/- y-plane offsets were both simulated due to the asymmetry in the y- plane due to the feedline and tuning stub in the + y-plane. However, since symmetry exists in the x-plane, only the + x-plane offset was simulated. The results of these simulations indicate that the worst-case photoetching misalignment should very minimally affect the performance of the wafer-scale patch antenna. The only notable effect seemed to be a +100 MHz center frequency shift with the +5 µm y-plane offset, which may partially be attributed to the model meshing variability between this simulation and that of the perfectly-aligned model and may also result from more of the feedline / tuning stub being shifted under the patch. The bandwidth, peak gain and HPBW remained minimally affected, with approximately the same values for the misaligned cases as those for the perfectly-aligned case.

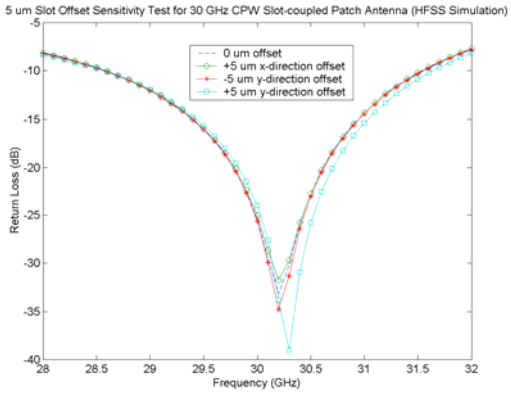

Fig. 11. HFSS-simulated S_{11} of wafer-scale patch antenna with 5 µm slot misalignment.

Next, this sensitivity test was expanded to discover approximately how misaligned the patch antenna and CPW feedline and slot must be in order to have a significant effect on antenna performance. The CPW feedline and slot were both offset from their centered position under the patch antenna at increments of ~54.5 µm in the + x-plane and at larger increments in the +/- y-plane up to the point where no part of the slot resided under the patch.

The results of the x-plane sensitivity test are shown in Fig. 12. These data indicates that a misalignment smaller than ~400 µm should yield a small (~0 to 100 MHz) center frequency shift and a bandwidth reduction down to ~6.5 – 7% (from its original 9.8% value). A misalignment greater than 400 µm may yield a significant return loss increase and consequential loss of resonance. Beyond 550 µm misalignment, the return loss increases above 10 dB for the entire 28 – 32 GHz frequency region of interest.

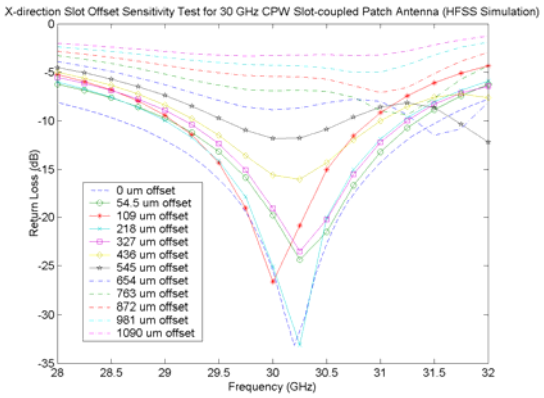

Fig. 12. HFSS-simulated S_{11} for wafer-scale patch antenna x-direction slot alignment sensitivity test.

The results of the y-plane sensitivity test are shown in Fig. 13. These data indicates that misalignment smaller than ~250 µm yields a small (~0 to 100 MHz) center frequency shift and a bandwidth reduction down to ~5.7 – 6.0 % (from its original 9.8 % value). A misalignment greater than 250 µm yields a significant return loss increase and loss of resonance. Beyond 400 µm misalignment, the return loss increases above 10 dB for the entire 28 – 32 GHz frequency region of interest.

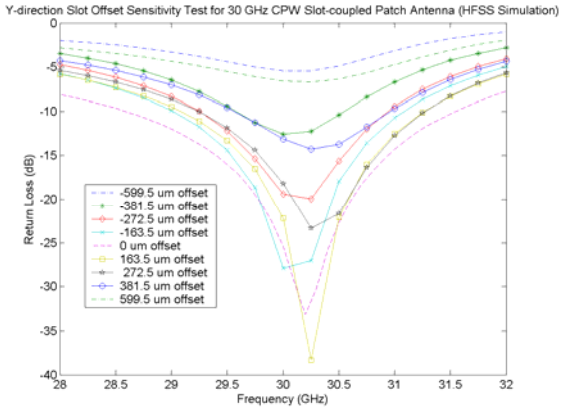

Fig. 13. HFSS-simulated S_{11} for wafer-scale patch antenna y-direction slot alignment sensitivity test.

From these results, the antenna performance is shown to be more sensitive to misalignment in the y-plane, with loss of resonance occurring at a misalignment ~150 µm smaller in the y-plane than in the x-plane. Another notable performance difference between x and y-plane misalignment is that the patch antenna bandwidth appears to be more critically affected by small y-plane misalignment than by x-plane misalignment, suffering a 0.8 – 1.0 % further decrease in bandwidth. Thus, according to these simulation results, a fabrication error of 300 – 400 µm or smaller in the x-plane or 200 – 300 µm or smaller in the y-plane should only cause a small % loss of bandwidth and should minimally affect the antenna resonance at 30 GHz. A very rare photo mask misalignment in the photoetching process could potentially bring about a slot/patch antenna misalignment greater than 300 – 500 µm, but with regards to the more common 0 – 5 µm-range fabrication errors, these tests have shown that the performance of this wafer-scale patch antenna design is considerably robust to slot misalignment.

VI. CONCLUSIONS

A coplanar waveguide slot-coupled K_a-band patch antenna has been successfully designed, constructed and tested for integration with a wafer-scale MEMS-switched antenna array beam-steering control board. HFSS simulation results show a 10 dB return loss bandwidth of 2.96 GHz (9.8 %) with a 4.6 dB peak gain and 110° HPBW. A scaled prototype at 6 GHz that was constructed on RT/Duroid 6010 substrate ($\varepsilon_r \approx 10.2$) yielded a

measured bandwidth of 360 MHz (6.0 %) and a peak gain of 4 dB. The measured bandwidth is nearly double the achieved bandwidth of existing single-substrate CPW-fed slot-coupled patch antenna designs and the promising simulation results for the wafer-scale design indicates the potential for bandwidth improvement of up to 4 times that of previously-reported designs.

The results from a wafer-scale fabrication error sensitivity test indicated that a CPW feedline / slot misalignment less than 200-400 μm should produce minimal degradation of antenna functionality, with the most significant impact being a 2.5 – 4.0 % drop in the antenna bandwidth and a small shift in the center frequency of 100 MHz or less. With wafer-scale fabrication errors on the order of less than 5 μm, the performance of this antenna design should be minimally affected by such circumstances. From this, it may be inferred that the production yield for a final wafer-scale integrated antenna array and MEMS beam-steering control board will not be significantly impacted by the antenna design and will mainly be dependent upon the MEMS switching element yield percentage.

The successful design and implementation of this patch antenna demonstrates a compact, efficient method for integration of a CPW slot-coupled K_a-band patch antenna onto a wafer-scale MEMS-switched control board without the need for additional substrate layers or feedline interconnects. This, in turn, minimizes the total system weight and decreases the wafer-scale fabrication complexity, yielding a lightweight, cost-effective solution for a microwave electronic scanning array for satellite communication.

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